

Electronic Applications

An Online Text

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Dedication

Human beings are a delightful and complex amalgam of the spiritual, the emotional, the intellectual, and the physical.

This is dedicated to all of them, especially to those who honor and nurture me with their friendship and love.

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Preface

Philosophy of an Online Text

I think of myself as an educator rather than an engineer. And it has long seemed to me that, as educators, we should endeavor to bring to the student not only as much information as possible, but we should strive to make that information as accessible as possible, and as inexpensive as possible.

The technology of the Internet and the World Wide Web now allows us to virtually *give away* knowledge! Yet, we don't, choosing instead to write another conventional text book, and print, sell, and use it in the conventional manner. The "whys" are undoubtedly intricate and many; I offer only a few observations:

- Any change is difficult and resisted. This is true in the habits we form, the tasks we perform, the relationships we engage. It is simply easier not to change than it is to change. Though change is inevitable, it is not well-suited to the behavior of any organism.
- The proper reward structure is not in place. Faculty are supposedly rewarded for writing textbooks, thereby bringing fame and immortality to the institution of their employ.¹ The recognition and reward structure are simply not there for a text that is simply "posted on the web."
- No economic incentive exists to create and maintain a

¹I use the word "supposedly" because, in my view, the official rewards for textbook authoring fall far short of what is appropriate and what is achievable through an equivalent research effort, despite all the administrative lip service to the contrary. These arguments, though, are more appropriately left to a different soapbox.

structure that allows all authors to publish in this manner; that allows students easy access to all such material, and that rigorously ensures the material will exceed a minimum acceptable quality.

If I were to do this the way I think it ought to be done, I would have prepared the course material in two formats. The first would be a text, identical to the textbooks with which you are familiar, but available online, and intended to be used in printed form. The second would be a slide presentation, à la Corel® Presentations™ or Microsoft® PowerPoint®, intended for use in the classroom or in an independent study.

But, alas, I am still on that journey, so what I offer you is a hybrid of these two concepts: an online text somewhat less verbose than a conventional text, but one that can also serve as classroom overhead transparencies.

Other compromises have been made. It would be advantageous to produce *two* online versions - one intended for use in printed form, and a second optimized for viewing on a computer screen. The two would carry identical information, but would be formatted with different page and font sizes. Also, to minimize file size, and therefore download times, font selection and variations are somewhat limited when compared to those normally encountered in a conventional textbook.

You may also note that exercise problems are not included with this text. By their very nature problems quickly can become “worn out.” I believe it is best to include problems in a separate document.

Until all of these enhancements exist, I hope you will find this a suitable and worthwhile compromise.

Enough of this; let’s get on with it...

Notes for Printing This Document

This document can be printed directly from the Acrobat® Reader - see the Acrobat® Reader help files for details.

If you wish to print the entire document, you may wish to do so in two sections, as most printer drivers will only spool a maximum of 255 pages at one time.

Copyright Notice and Information

This entire document is ©1999 by Bob Zulinski. All rights reserved.

I copyrighted this online text because it required a lot of work, and because I hold a faint hope that I may use it to acquire immeasurable wealth, thereby supporting the insatiable, salacious lifestyle that I've always dreamed of.

Thus, you will need my permission to print it. You may obtain that permission simply by asking: tell me who you are and what you want it for. Route your requests via email to rzulinsk@mtu.edu, or by USPS mail to Bob Zulinski, Dept. of Electrical Engineering, Michigan Technological University, Houghton MI 49931-1295.

Generous monetary donations included with your request will be looked upon with great favor.

Thermal Considerations in Amplifiers

In every amplifier, some power is dissipated as heat, thus, some form of heat removal is required.

In power amplifiers heat is significant, and heat sinks are required:



Fig. 1. Examples of heat sinks. Clockwise from top: power supply heat sink with two TO-3 case-style BJTs; pressure-fit heat sink over TO-5 case-style BJT; heat sink with TO-220 case-style BJT.

Junction Temperature, T_J

Most of the device dissipation occurs at the collector-base junction.

The device/chip must be operated below a specified $T_{J\max}$.

Typically,

- $T_{J\max} = 200\text{ }^{\circ}\text{C}$ (silicon devices in metal cases)
- $T_{J\max} = 150\text{ }^{\circ}\text{C}$ (silicon devices in plastic cases)

Thermal Resistance

Heat flows between any two points X and Y if a temperature difference exists between them.

The steady-state temperature difference is proportional to the thermal power.

Our immediate concern is with electronic devices:

- Heat flow: Junction → Case → Heat Sink → Ambient Air
- The power dissipated in the device is the thermal power.

In steady-state, we have the generic equation:

$$T_X - T_Y = P_D \theta_{XY} \quad (1)$$

where: T_X and T_Y are the temperatures at points X and Y,
 P_D is the power dissipated in the device, and
 θ_{XY} is the **thermal resistance** between X and Y.

Note that the units of θ_{XY} are °C/W or K/W.

Also note the similarity of eq. (1) to Ohm's Law: $V = IR \dots$

We can construct a “thermal circuit” that is analogous to an electrical circuit!!!

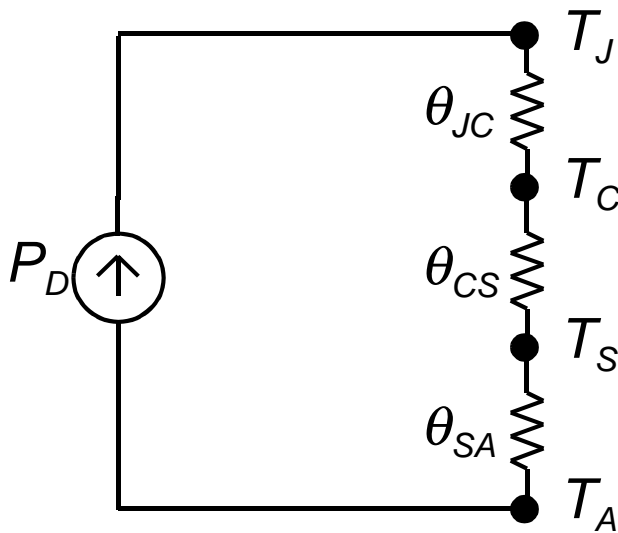


Fig. 2. Heat flow circuit analogy.

In constructing a thermal circuit, we use subscripts to indicate:

Junction temperature,

Case temperature,

Sink temperature, and

Ambient temperature.

As with electrical circuits:

$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \quad (2)$$

Specifying Device Ratings

Various manufacturers use various methods.

Power Derating Curves:

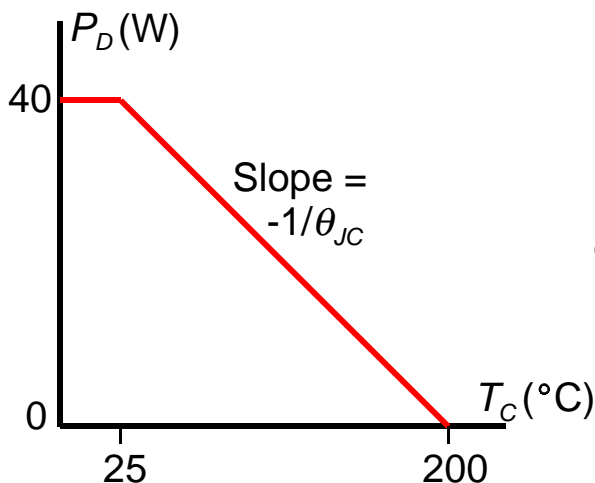


Fig. 3. Power derating curve example.

This is a plot of allowable power dissipation vs. case temperature. In this example $T_{J\max} = 200^\circ\text{C}$, and

$$\begin{aligned} \theta_{JC} &= \frac{T_J - T_C}{P_D} = \frac{200^\circ\text{C} - 25^\circ\text{C}}{40\text{ W}} \\ &= 4.38 \frac{^\circ\text{C}}{\text{W}} \end{aligned} \quad (3)$$

Sometimes T_A is used rather than T_C . Then:

$$\theta_{JA} = \frac{T_J - T_A}{P_D} \quad (4)$$

Device Maximum Ratings:

Some manufacturers just give $T_{J\max}$ and $P_{D\max}$, e.g.,

$$\text{“ } T_{J\max} = 150\text{ }^{\circ}\text{C} \text{ and } P_{D\max} = 15\text{ W at } T_C = 25\text{ }^{\circ}\text{C} \text{ ”}$$

For this example, then:

$$\theta_{JC} = \frac{T_J - T_C}{P_D} = \frac{150\text{ }^{\circ}\text{C} - 25\text{ }^{\circ}\text{C}}{15\text{ W}} = 8.33 \frac{^{\circ}\text{C}}{\text{W}} \quad (5)$$

Thermal Resistance, Junction-to-Case

For lowest θ_{JC} the collector (or drain) is often in direct electrical and thermal contact with the metal case.

The circuit designer's only influence on θ_{JC} is in choosing an appropriate device.

Thermal Resistance, Case-to-Sink

Designer's influence on θ_{CS} :

- Choosing device with the desired type of case.
- Applying a thermally-conductive compound between case and sink.
- Because the collector (or drain) is usually electrically connected to the case, and the *collector is not usually at ground potential*:

The case must be electrically insulated from the sink (usually with a washer of mica or similar material), or

The sink must be electrically insulated from the chassis (usually not done - *can be very dangerous*),

- Without additional information, it is usually assumed that $\theta_{CS} \cong 1 \text{ }^{\circ}\text{C/W}$.

Thermal Resistance, Sink-to-Ambient

The designer's influence on θ_{SA} is by selection of heat sink.

Heat sinks range . . .

- . . . from none (device case is the heat sink),
- . . . to clip-on units,
- . . . to large extruded aluminum units,
- . . . to forced-air cooled arrangements,
- . . . to water-cooled copper units.

Reference

For an *excellent* and thorough technical description of extruded, fabricated, and water-cooled heat sinks, download the catalogs [*sic*] from R-Theta[®] Corporation of Mississauga, Ont.

They are available via links at:

<http://www.r-theta.com/products/info.html>

Power Devices

Power BJT vs. Small-Signal BJT

Power devices have lower β , e.g., $\beta \approx 10$ vs. $\beta \approx 100$.

Power devices require larger collector area due to the higher P_D , thus:

- The internal capacitances are larger.
- The transition frequency (f_T) is lower.
- The reverse leakage current (I_{CBO}) is higher.

Effect of Temperature on BJTs

As temperature increases:

- β increases, approximately 3 times from -55°C to 150°C .
- I_{CBO} increases, approximately 2 times per 10°C rise.
- V_{BE} (for fixed I_C) decreases, $-2.5\text{ mV} / ^\circ\text{C}$.

As a result of these three effects, P_D increases, which further increases the junction temperature.

Thermal Runaway:

This describes the positive feedback process of higher T_J , higher P_D , higher T_J , etc., which eventually destroys the device.

BJT Safe Operating Area (SOA)

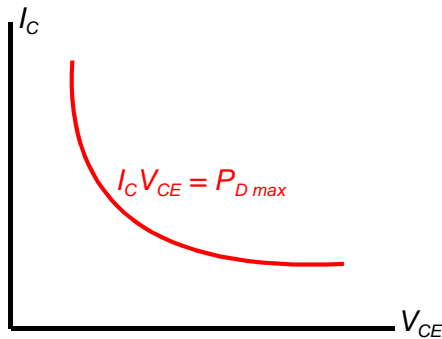


Fig. 4. BJT constant-power parabola.

The maximum power parabola, from $I_C V_{CE} = P_{D max}$, is plotted at left.

This becomes a straight line on a log-log plot, as we see from:

$$\log I_C + \log V_{CE} = \log P_{D max} \quad (6)$$

Using this and other restrictions on BJT operation gives rise to the BJT Safe Operating Area:

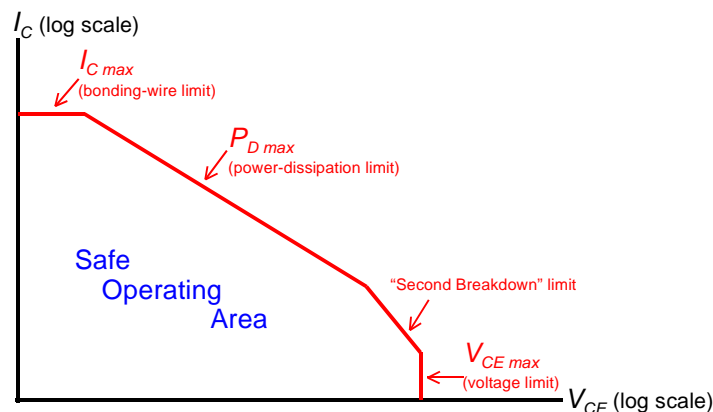


Fig. 5. BJT Safe Operating Area (usually specified at $T_C = 25^\circ\text{C}$).

Note that second breakdown results from localized “hot spots” at the collector-base junction, which then cause failure due to thermal runaway.

Power MOSFETs (Enhancement-Mode Only)

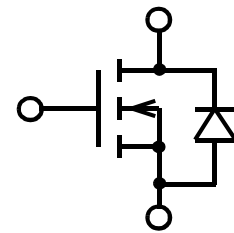
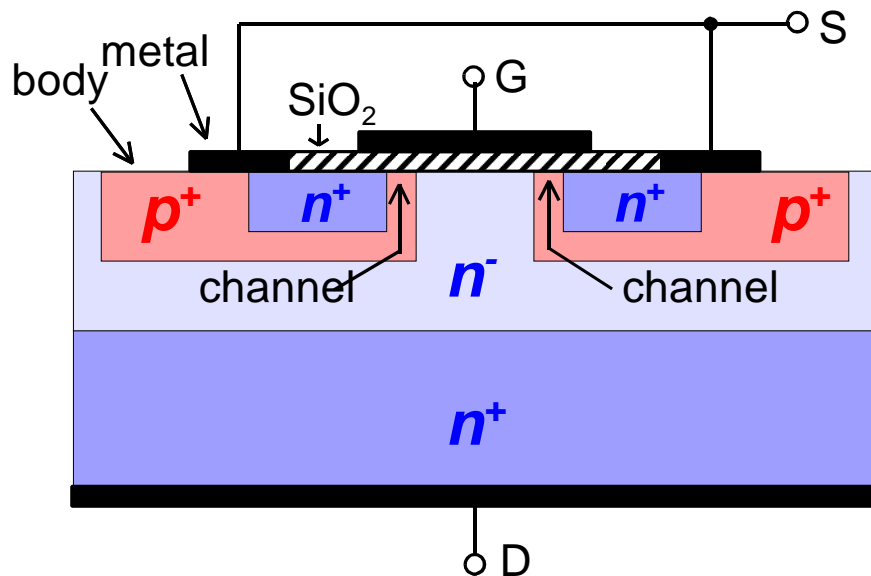


Fig. 7. Power MOSFET model.

Fig. 6. Illustration of power MOSFET cell construction. Many cells can be paralleled for higher power devices.

- Power MOSFETs are constructed “vertically” (low-power MOSFETs are constructed horizontally).
- Positive v_{GS} enhances the channel between source metalizations.
- Positive v_{DS} reverse biases the body-drain “parasitic” diode.
- Low channel resistance results from a short channel length, and a heavily doped n^+ substrate.
- High breakdown voltage results from a lightly doped n^- region.

Power MOSFET Characteristics

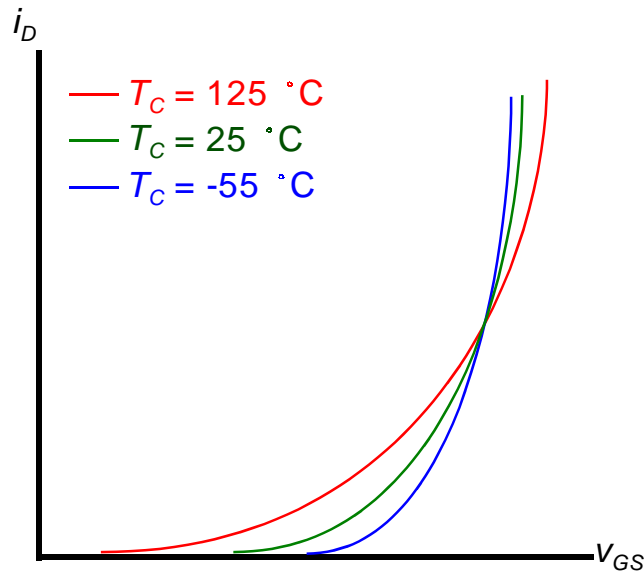


Fig. 8. Power MOSFET transfer characteristics.
Note point of zero temperature coefficient.

- Can be biased with zero temperature coefficient.
- Very low static drive requirements (can be logic driven).
- Lower switching times than BJT (no minority carriers, no stored charge).
- At large I_D , I_D decreases with temperature - no thermal runaway.
- No second breakdown.

Power Amplifiers

Introduction

Basically, power amplifiers are used to amplify two types of signals:

- Baseband → f_H/f_L large → audio, video
- Bandpass → f_H/f_L small → communication systems

Power amplifiers also fall into many different “classes” of operation:

- Class A → devices in active region always ($\theta_{cond} = 360^\circ$)
suitable for baseband or bandpass signals
 - Class B → devices active for half cycle ($\theta_{cond} = 180^\circ$)
suitable for baseband or bandpass signals,
depending on the amplifier configuration
 - Class C → devices active < half cycle ($\theta_{cond} < 180^\circ$)
suitable for bandpass signals only
 - Class D → devices act as switches
suitable for baseband or bandpass signals,
depending on the amplifier configuration
 - Class E → devices act as switches
suitable for bandpass signals only
 - Other, less-common, classes with specialized uses, e.g.,
Class F, Class G, Class H, Class S.
-

Calculating Power Dissipation

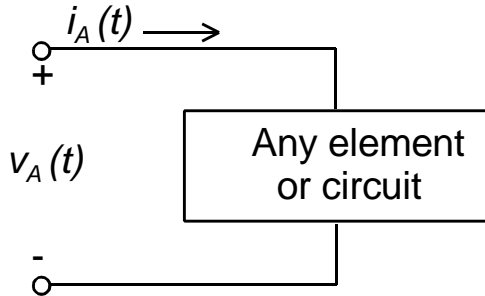


Fig. 9. Calculating power.

Instantaneous power:

$$p_A(t) = v_A(t)i_A(t) \quad (7)$$

We usually assume that the amplifier signals are periodic to simplify calculations.

The energy delivered per cycle for a periodic signal is:

$$E_A = \int_0^T p_A(t)dt = \int_0^T v_A(t)i_A(t)dt \quad (8)$$

And the average power delivered is:

$$P_A = \frac{E_A}{T} = \frac{1}{T} \int_0^T v_A(t)i_A(t)dt \quad (9)$$

For a constant voltage source, the average power delivered is:

$$P_{CC} = \frac{1}{T} \int_0^T V_{CC}i_{CC}(t)dt = V_{CC} \frac{1}{T} \int_0^T i_{CC}(t)dt = V_{CC}I_{CC} \quad (10)$$

Note that $I_{CC} = i_{CC \text{ average}}$, which is the dc component of $i_{CC}(t)!!!$

For a constant current source we also obtain $P_{CC} = V_{CC}I_{CC}$, except in this case V_{CC} is the average, or dc component, of $v_{CC}(t)$.

Amplifier Performance Measures

Efficiency:

Efficiency is almost always expressed as a percentage:

$$\eta = \frac{\text{signal power delivered to load}}{\text{total power delivered by dc sources}} = \frac{P_o}{P_{IN}} \quad (11)$$

Power Capability:

Power capability is a measure of how much signal power I can deliver to a load with a specific device:

$$C_P = \frac{P_{O_{max}}}{V_{CE_{max}} i_{C_{max}}} \quad (12)$$

where, $P_{O_{max}}$ = maximum possible output power,

$V_{CE_{max}}$ = maximum device voltage throughout cycle

$i_{C_{max}}$ = maximum device current throughout cycle

Class A Integrated-Circuit Power Amplifier

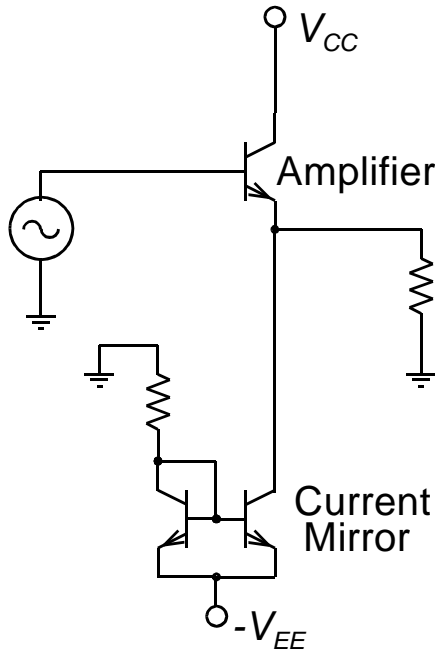


Fig. 10. IC Class A amplifier.

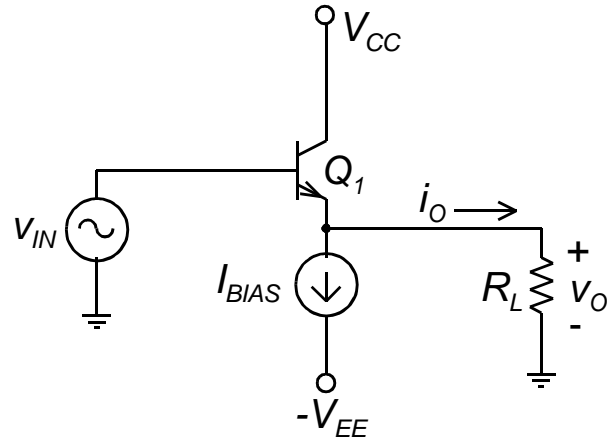
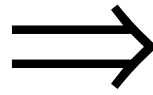


Fig. 11. Generic class A amplifier, equivalent to Fig. 10.

Note that Q_1 is an emitter follower. Thus, it has low Z_{out} , high A_i , high G , and unity A_v .

Class A Analysis:

We use two assumptions to simplify the analysis:

$$V_{CE_{sat}} = 0 \quad \text{and} \quad V_{BE_{fwd}} = 0 \quad (13)$$

Now, when v_{IN} swings positive (and keeping Q_1 from saturation):

$$v_{O_{max}} = V_{CC} \quad \text{and} \quad i_{O_{max}} = \frac{V_{CC}}{R_L} \quad (14)$$

Thus:

$$i_{C1_{max}} = I_{BIAS} + \frac{V_{CC}}{R_L} \quad (15)$$

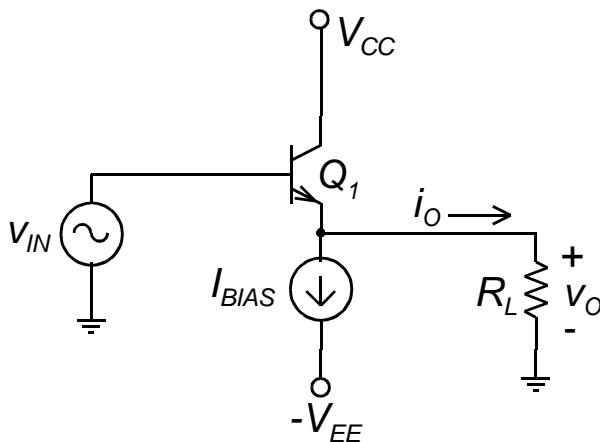


Fig. 12. Class A amplifier (Fig. 11 repeated).

Now, when v_{IN} swings negative, $v_{O\min}$ depends on whether:

Q_1 reaches cutoff first, or

Q_3 reaches saturation first.

(Q_3 is the current mirror output transistor.)

If Q_1 reaches cutoff first:

$$i_{C1} = 0 \quad i_{O\min} = -I_{BIAS} \quad v_{O\min} = -I_{BIAS} R_L \quad (16)$$

For Q_1 to reach cutoff before Q_3 reaches saturation, $v_{O\min} > -V_{EE}$.

If Q_3 reaches saturation first:

$$v_{O\min} = -V_{EE} \quad i_{O\min} = -\frac{V_{EE}}{R_L} \quad i_{C1} = I_{BIAS} - \frac{V_{EE}}{R_L} \quad (17)$$

For Q_3 to reach saturation before Q_1 reaches cutoff, $I_{BIAS} > V_{EE}/R_L$.

Q. How can obtain maximum negative swing, without excessive I_{BIAS} ?

A. If we design the circuit so that Q_1 reaches the edge of cutoff and Q_3 reaches the edge of saturation **at the same instant !!!**
We can do this if we choose, by design:

$$I_{BIAS} = \frac{V_{EE}}{R_L} \quad (18)$$

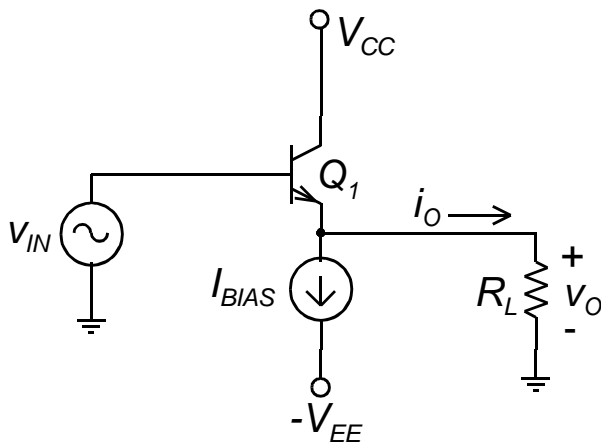


Fig. 13. Class A amplifier (Fig. 11 repeated).

Class A Waveforms:

In most class A circuits

$$|V_{CC}| = |V_{EE}| \quad (19)$$

which allows these maximum-amplitude waveforms:

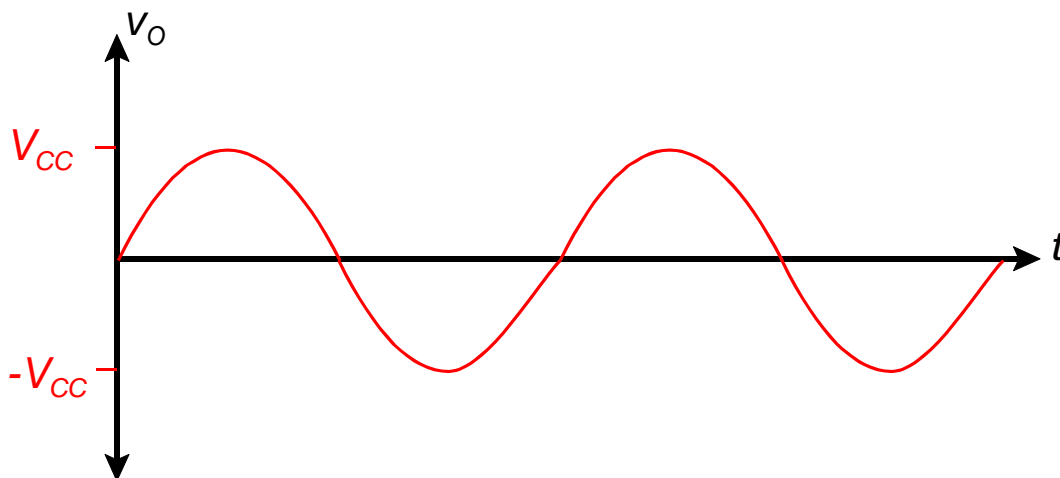


Fig. 14. Maximum output voltage magnitude in class A amplifier. Source v_{IN} must be capable of producing this amplitude.

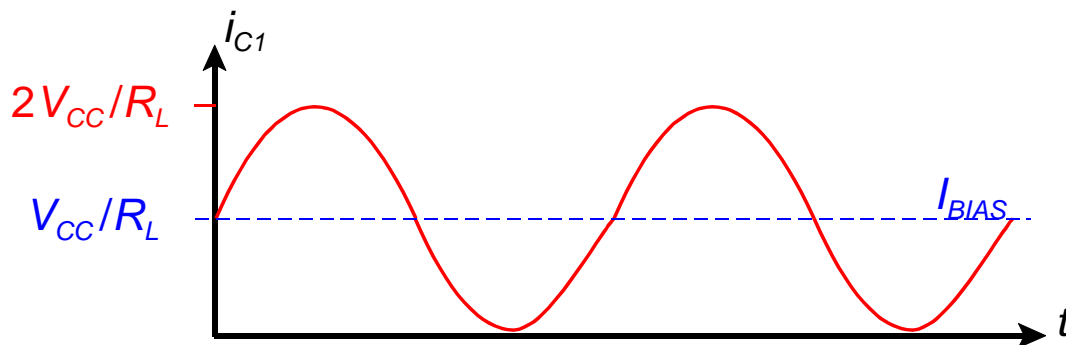


Fig. 15. Collector current in Class A amplifier with maximum output voltage.

Class A Calculations:

1. Output Power

Recall that $v_o \approx v_{IN}$. Usually, we assume that $v_o = V_m \sin \omega t$.

Because $V_{m \max} = V_{CC}$, we have:

$$P_o = \frac{V_m^2}{2R_L} \quad \text{and} \quad P_{o_{\max}} = \frac{V_{CC}^2}{2R_L} \quad (20)$$

2. DC Supply Power

This is more typically called *input power*, P_{in} . From eqs. (10) and (18) we have for the positive supply, V_{CC} :

$$P_{CC} = V_{CC} I_{CC} = V_{CC} \left(\frac{V_{CC}}{R_L} \right) = \frac{V_{CC}^2}{R_L} \quad (21)$$

Similarly, for the negative supply, V_{EE} :

$$P_{EE} = V_{EE} I_{BIAS} = V_{CC} \left(\frac{V_{CC}}{R_L} \right) = \frac{V_{CC}^2}{R_L} \quad (22)$$

Thus:

$$P_{in} = P_{CC} + P_{EE} = \frac{2V_{CC}^2}{R_L} \quad (23)$$

3. Efficiency

$$\eta = \frac{P_o}{P_{in}} = \frac{V_m^2 / 2R_L}{2V_{CC}^2 / R_L} = 0.25 \left(\frac{V_m}{V_{CC}} \right)^2 \quad (24)$$

$$\text{Thus:} \quad \eta_{\max} = 25\% \quad (25)$$

4. Power Capability

$$C_P = \frac{P_{o_{\max}}}{V_{CE_{\max}} i_{C_{\max}}} = \frac{V_{CC}^2 / 2R_L}{(2V_{CC})(2V_{CC} / R_L)} = 0.125 \quad (26)$$

5. Transistor Power Dissipation

Because the voltage across it is small, the power dissipated in the current mirror reference transistor ≈ 0 .

The power dissipated in the current mirror output transistor:

$$P_{\text{mirror}} = V_{BIAS} I_{BIAS} = V_{EE} I_{BIAS} = \frac{V_{CC}^2}{R_L} \quad (27)$$

where V_{BIAS} is the average voltage across " I_{BIAS} ."

Finally, the power dissipated in amplifier transistor is:

$$P_{Q_1} = P_{in} - P_{\text{mirror}} - P_o = \frac{2V_{CC}^2}{R_L} - \frac{V_{CC}^2}{R_L} - \frac{V_m^2}{2R_L} = \frac{V_{CC}^2 - \frac{V_m^2}{2}}{R_L} \quad (28)$$

from which:

$$P_{Q_{1\max}} = \frac{V_{CC}^2}{R_L} \quad \text{when} \quad V_m = 0 \quad (29)$$

and

$$P_{Q_{1\min}} = \frac{V_{CC}^2}{2R_L} \quad \text{when} \quad V_m = V_{CC} \quad (30)$$

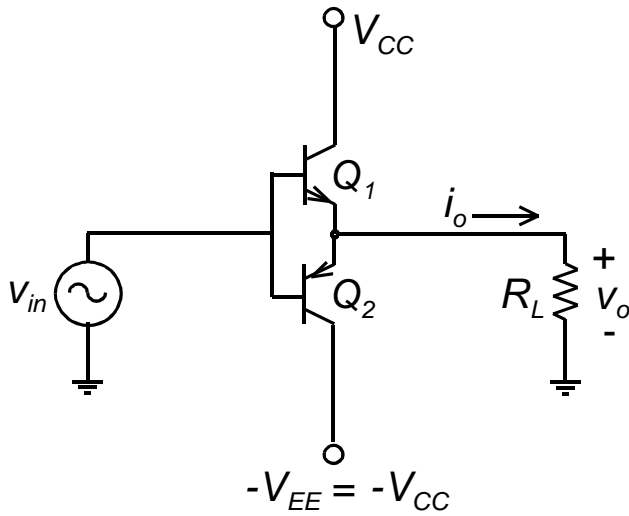


Fig. 16. Class B complementary amplifier.

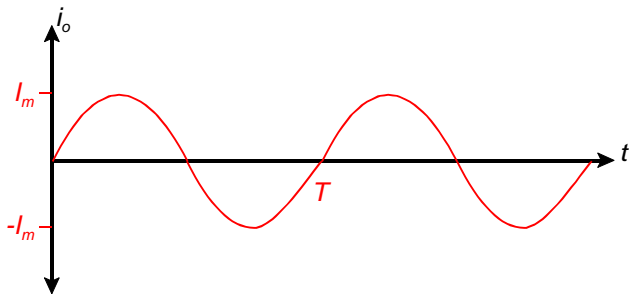
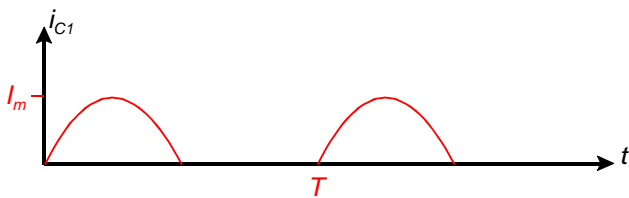
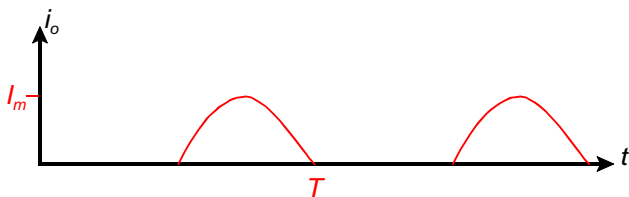


Fig. 17. Class B output current.

Fig. 18. Q_1 collector current.Fig. 19. Q_2 collector current.

Class B Complementary Amplifier

“Complementary” means that we have npn and pnp devices with identical characteristics.

It is not critical that these devices be truly complementary.

Q_1 is active on positive half-cycles; Q_2 is active on negative half-cycles.

Class B Analysis:

We begin the analysis with the idealizing assumptions:

$$V_{CE_{sat}} = 0$$

$$V_{BE_{fwd}} = 0 \quad (31)$$

$$i_C = i_E$$

We further assume input and output are sinusoidal, and use some notational convenience:

$$v_o(t) = V_m \sin \omega t = V_m \sin \theta$$

$$i_o(t) = \frac{V_m}{R_L} \sin \omega t = I_m \sin \theta \quad (32)$$

Class B Calculations:

1. Output Power

This is the familiar result obtained with a sinusoidal voltage across a purely resistive load:

$$P_o = \frac{V_m^2}{2R_L} \quad \text{and} \quad P_{o_{\max}} = \frac{V_{CC}^2}{2R_L} \quad (33)$$

2. Input Power

For the power delivered by the positive supply we need the average current through Q_1 . This is just the average of a half-wave-rectified waveform:

$$P_{CC} = V_{CC} I_{CC} = V_{CC} \left(\frac{I_m}{\pi} \right) = \frac{V_{CC} V_m}{\pi R_L} \quad (34)$$

We have a similar result for the power delivered by the negative supply:

$$P_{EE} = V_{EE} I_{EE} = V_{CC} \left(\frac{I_m}{\pi} \right) = \frac{V_{CC} V_m}{\pi R_L} \quad (35)$$

And the total input power is the sum of these two:

$$P_{in} = P_{CC} + P_{EE} = \frac{2V_{CC} V_m}{\pi R_L} \quad (36)$$

3. Efficiency

$$\eta = \frac{P_o}{P_{in}} = \frac{V_m^2 / 2R_L}{2V_{CC} V_m / \pi R_L} = \frac{\pi}{4} \left(\frac{V_m}{V_{CC}} \right) \quad (37)$$

Because V_m cannot be greater than V_{CC} (Q_1 cannot become saturated):

$$\eta_{\max} = \frac{\pi}{4} = 78.5\% \quad (38)$$

4. Power Capability

$$c_P = \frac{P_{o_{\max}}}{V_{CE_{\max}} i_{C_{\max}}} = \frac{V_{CC}^2 / 2R_L}{(2V_{CC})(V_{CC} / R_L)} = 0.25 \quad (39)$$

Because there are two devices, $c_p = 0.125$ per device . . . the same as in the Class A amplifier.

5. Transistor Power Dissipation

The difference between input and output power must be dissipated in the devices:

$$P_{DQ1} + P_{DQ2} = P_{in} - P_o = \frac{2V_{CC} V_m}{\pi R_L} - \frac{V_m^2}{2R_L} \quad (40)$$

From symmetry we can conclude $P_{DQ1} = P_{DQ2}$, but how do we determine the maximum dissipation, $P_{DQ \max}$???

To find $P_{DQ\ max}$, we set the derivative of (40) to zero:

$$\frac{\partial (P_{DQ1} + P_{DQ2})}{\partial V_m} = 0 \quad (41)$$

from which

$$P_{DQ1\ max} = P_{DQ2\ max} = \frac{2}{\pi^2} P_{o\ max} = \frac{V_{CC}^2}{\pi^2 R_L} \quad (42)$$

which occurs for

$$V_m = \frac{2V_{CC}}{\pi} \quad (43)$$

Various class B parameters are plotted in the figure below:

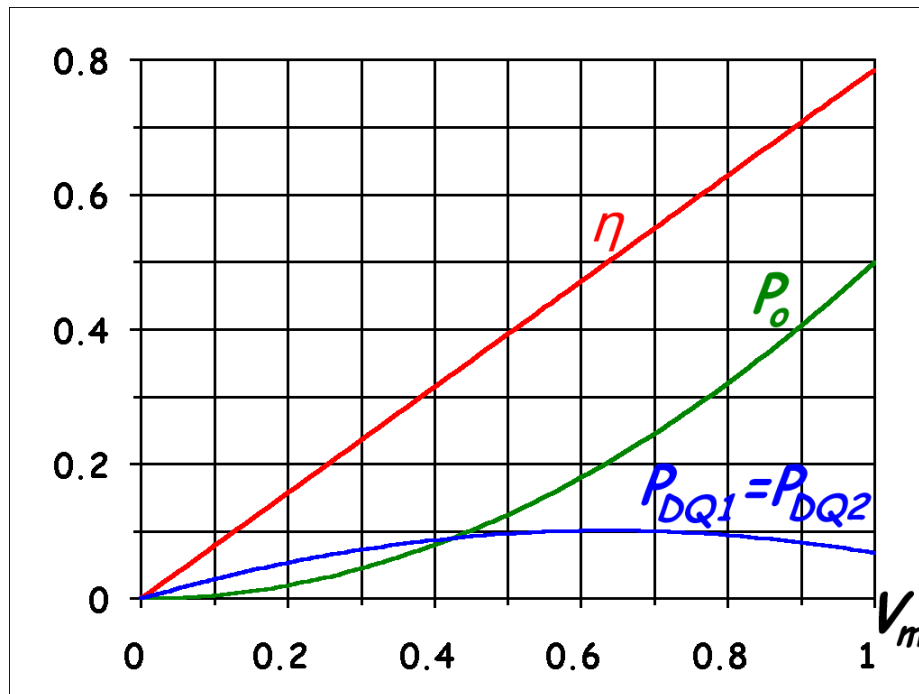


Fig. 20. Plots of efficiency, output power, and device dissipation for a class B amplifier with normalized values of $V_{CC} = 1\text{ V}$ and $R_L = 1\ \Omega$.

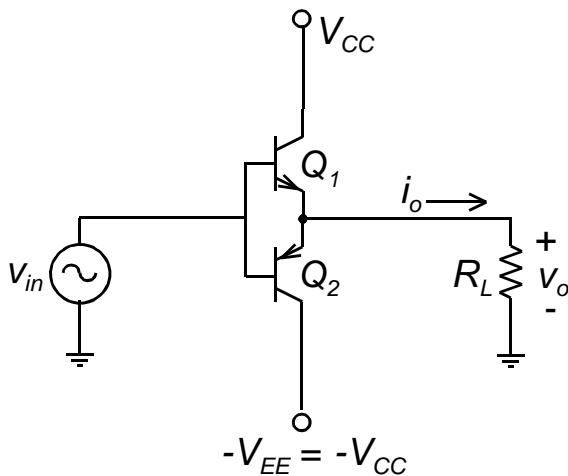


Fig. 21. Class B amp (Fig. 16 repeated).

Crossover Distortion:

In a real amplifier $v_{BE\text{ fwd}} = 0.7\text{ V}$ (not zero)!!!

So $v_o = 0$ for $|v_{in}| < 0.7\text{ V}$!!! The effect on the output voltage is called crossover distortion:

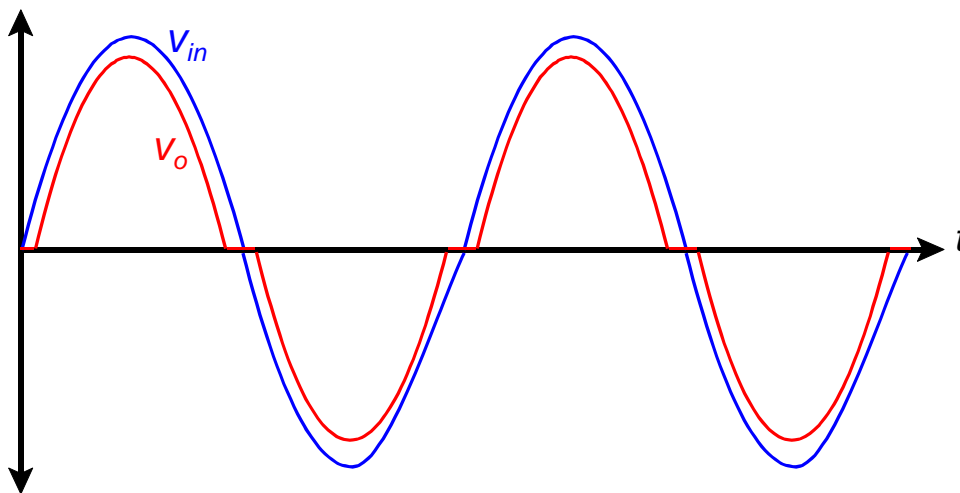


Fig. 22. Illustration of crossover distortion.

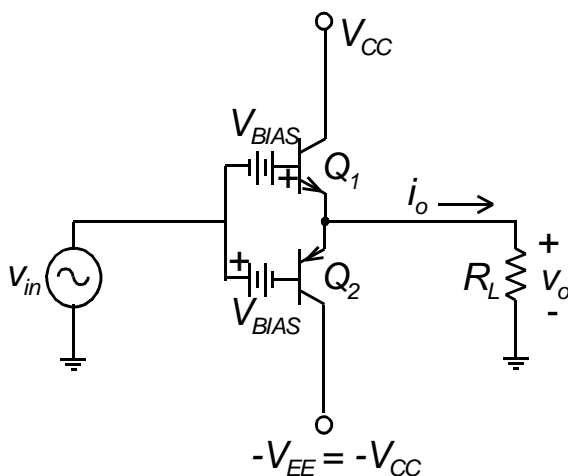


Fig. 23. Class AB amplifier.

Eliminating crossover distortion requires biasing slightly into the active region.

One approach is to add a small bias voltage, $V_{BIAS} \approx 0.7\text{ V}$.

The result is a “Class AB” amplifier. Details of various approaches are left to your curiosity.

Single-Ended Power Amplifiers

The term single-ended refers to a single active device, usually referenced to ground.

Class A Single-Ended Power Amplifier

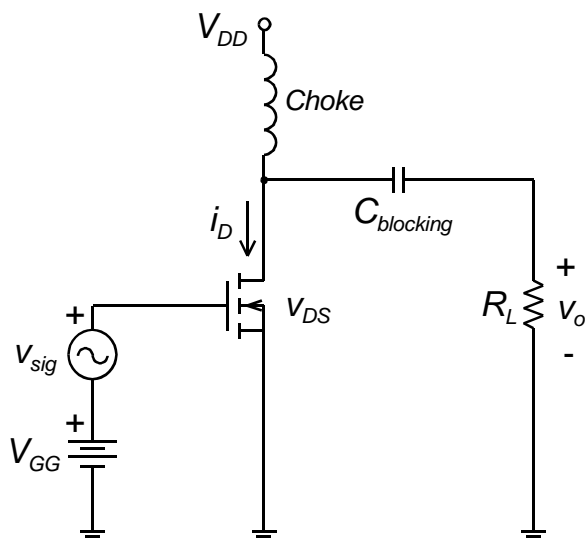


Fig. 24. Class A single-ended amplifier.

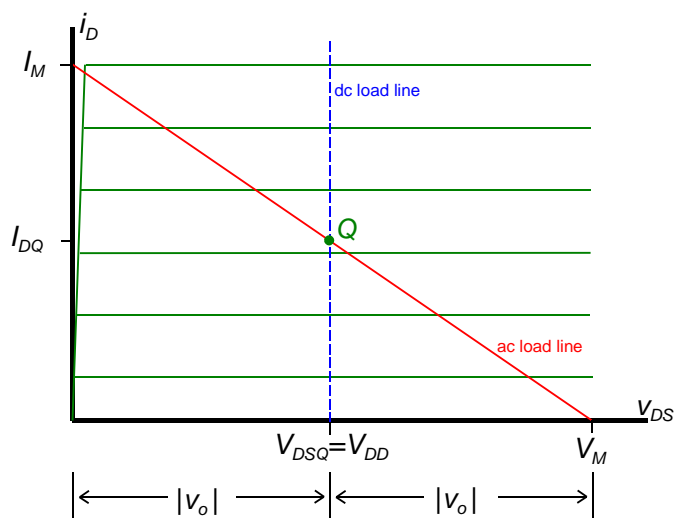


Fig. 25. FET output characteristics.

Circuit Operation:

Gate voltage V_{GG} is large enough so the FET is always in the pinch-off region (class A). For maximum output swing, the Q-point should be placed in the middle of the ac load line, as shown. (We determine the details of placing the Q-point later.)

The choke is a very large inductance, with essentially infinite impedance at the operating frequency, and zero impedance at dc. Thus only dc current can flow through choke!!!

The blocking capacitor is also very large, with infinite impedance at dc, and nearly zero impedance at the operating frequency. Thus only signal current (zero average) can flow through load!!!

These two form a frequency-sensitive current divider!!!

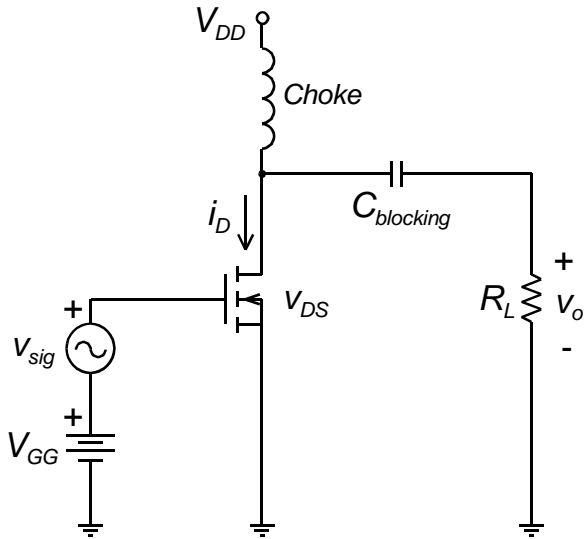


Fig. 26. Class A single-ended amplifier (Fig. 24 repeated).

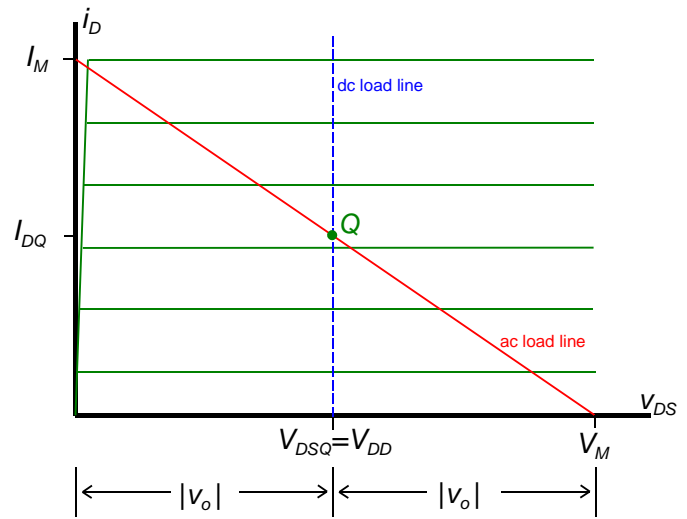


Fig. 27. FET output characteristics (Fig. 25 repeated).

From a study of Fig. 27, note that the maximum drain-source voltage is noted as V_M .

For a sinusoidal output (which we typically assume):

$$v_o = (V_M - V_{DD}) \sin \omega t = V_m \sin \theta \quad (44)$$

And, for maximum output swing:

$$V_M - V_{DD} = V_{DD} - 0 \quad \text{thus} \quad V_M \leq 2V_{DD} \quad (45)$$

Eq. (45) mathematically shows that Q must bisect the ac load line for maximum output swing *to be possible*. We would still need v_{sig} to be large enough to achieve maximum output swing.

Because R_L determines the slope of the ac load line, we can write:

$$I_M = \frac{V_M}{R_L} \quad \text{and} \quad I_{DQ} = \frac{V_M}{2R_L} \quad (46)$$

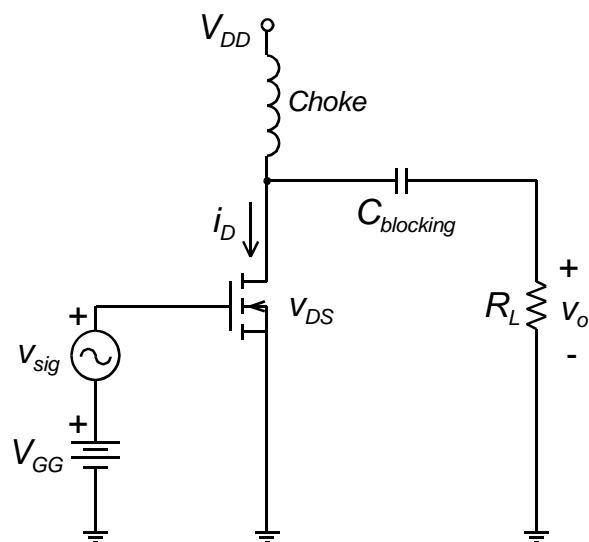


Fig. 28. Class A single-ended amplifier (Fig. 24 repeated).

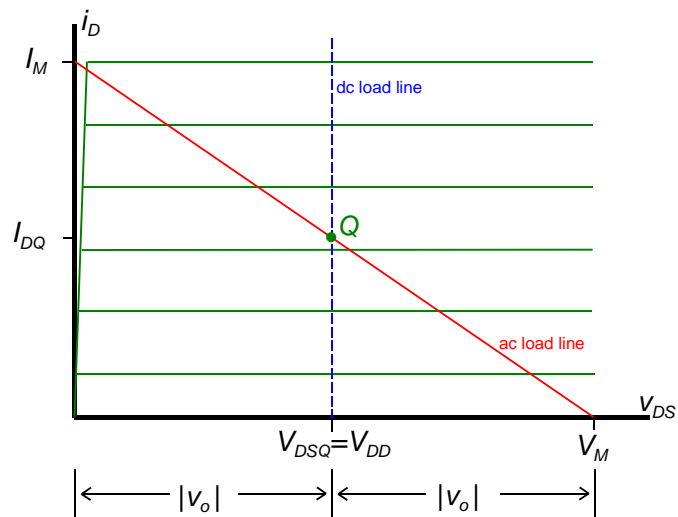


Fig. 29. FET output characteristics (Fig. 25 repeated).

To allow for maximum output amplitude, and thus maximum P_o :

$$I_{DQ} = \frac{V_{DD}}{R_L} \quad (47)$$

The bias voltage V_{GG} must be “adjusted” to achieve this I_{DQ} . A higher bias voltage would create a larger I_{DQ} , but could not provide for a larger output voltage. Thus it would only waste power.

Calculations:

1. Average Output Power

$$P_o = \frac{V_m^2}{2R_L} \quad \text{and} \quad P_{o_{\max}} = \frac{V_{DD}^2}{2R_L} \quad (48)$$

2. Average Input Power:

$$P_{in} = V_{DD} I_{DQ} = \frac{V_{DD}^2}{R_L}$$

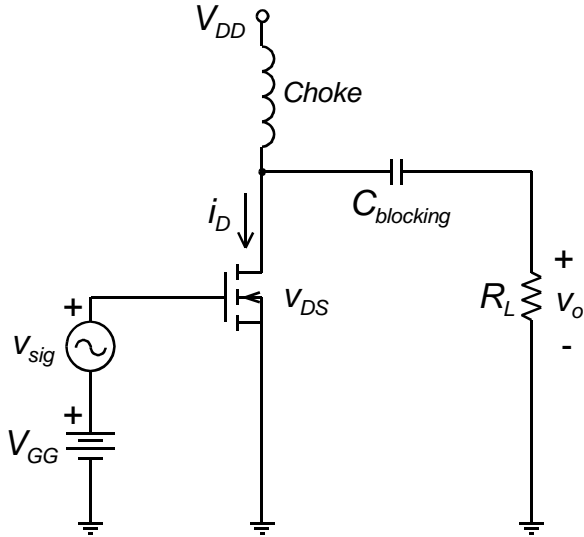


Fig. 30. Class A single-ended amplifier (Fig. 24 repeated).

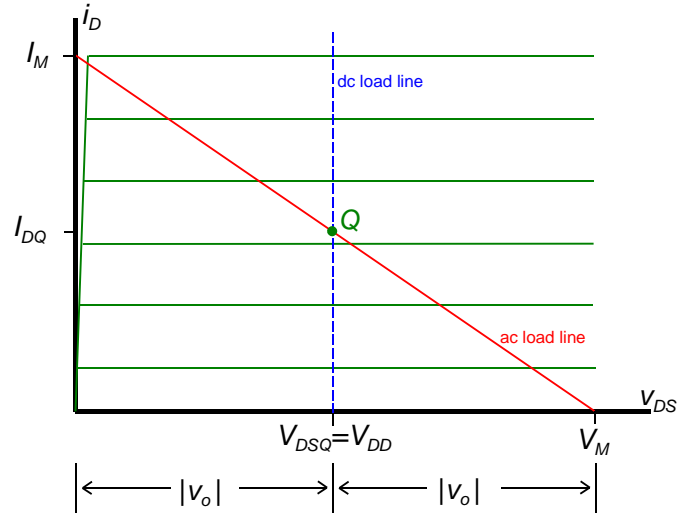


Fig. 31. FET output characteristics (Fig. 25 repeated).

3. Efficiency

$$\eta = \frac{P_o}{P_{in}} = \frac{V_m^2 / 2R_L}{V_{DD}^2 / R_L} = \frac{1}{2} \left(\frac{V_m^2}{V_{DD}^2} \right) \quad \text{thus} \quad \eta_{\max} = 50\% \quad (50)$$

4. Power Capability

$$c_P = \frac{P_{o_{\max}}}{V_{DS_{\max}} i_{D_{\max}}} = \frac{V_{DD}^2 / 2R_L}{(2V_{DD})(2V_{DD} / R_L)} = \frac{1}{8} = 0.125 \quad (51)$$

5. FET Power Dissipation

$$P_Q = P_{in} - P_o = \frac{V_{DD}^2}{R_L} - \frac{V_m^2}{2R_L} \quad (52)$$

$$P_{Q_{\min}} = \frac{V_{DD}^2}{2R_L} \quad \text{at} \quad P_o = P_{o_{\max}} \quad \text{and} \quad P_{Q_{\max}} = \frac{V_{DD}^2}{R_L} \quad \text{at} \quad P_o = 0 \quad (53)$$

Class B Single-Ended Amplifier

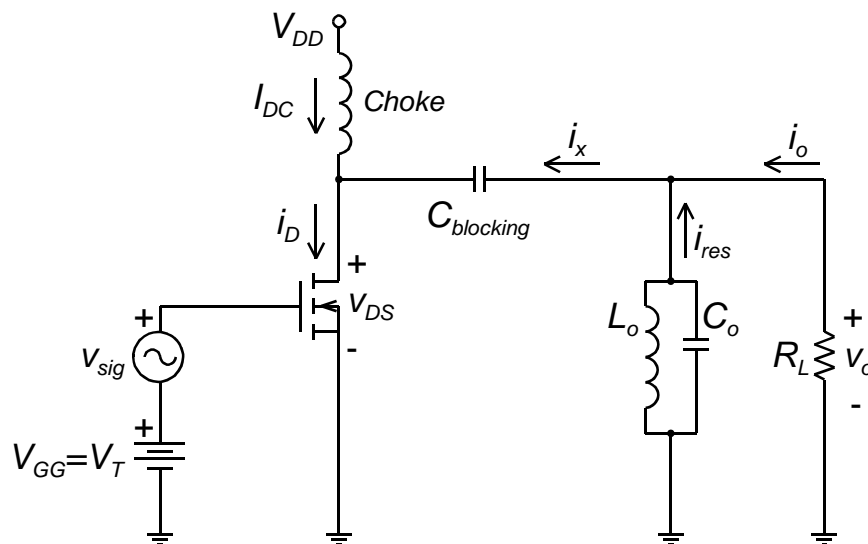


Fig. 32. Class B single-ended amplifier.

Circuit Operation:

This circuit is biased at the threshold voltage, so only positive half-cycles of the signal can move the device into the pinch-off region.

As we have done before, we let $\omega t = \theta$ for convenience.

Also as before, the choke has infinite impedance at the operating frequency, and zero impedance at dc. *Only dc current can flow through the choke !!!*

The blocking capacitor has infinite impedance at dc, and zero impedance at operating frequency. *Only signal current (zero average) can flow toward load !!!*

In addition, $L_o - C_o$ is a parallel resonant circuit. It has infinite impedance at the operating frequency, θ , and zero impedance (we assume) at all harmonics (2θ , 3θ , etc.). Thus:

- *All harmonic signal current flows through $L_o - C_o$, not R_L !!!*
- *Only fundamental signal current (at θ) flows through R_L !!!*

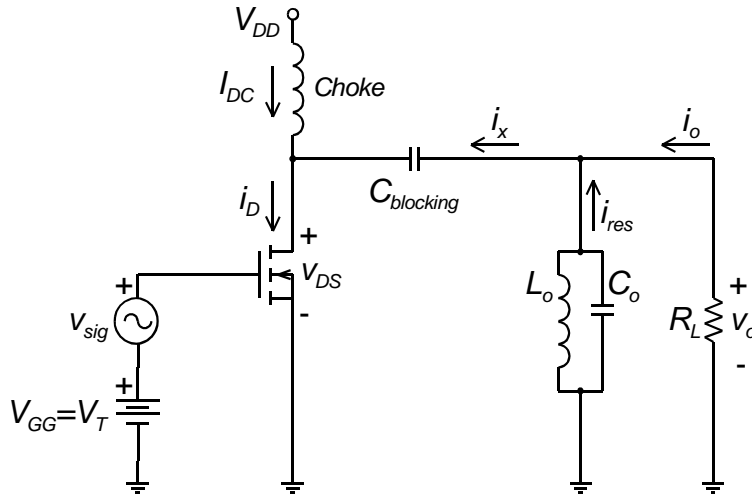


Fig. 33. Class B single-ended amplifier (Fig. 32 repeated).

To repeat, the FET is biased at V_T .

Thus it is in the cutoff region for $v_{sig} < 0$,

and in the pinch-off region for $v_{sig} > 0$.

We make the standard assumption: a sinusoidal input at θ :

$$v_{sig} = K \sin \omega t = K \sin \theta \quad (54)$$

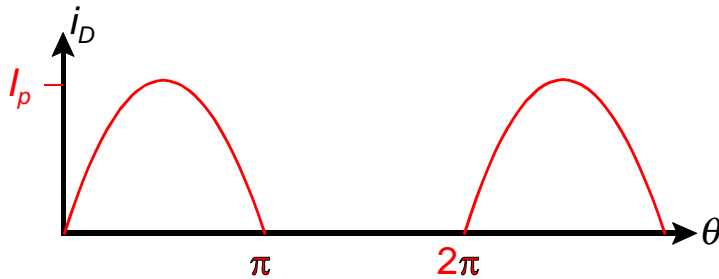


Fig. 34. Drain current in class B amplifier. The magnitude of the current pulses is yet undetermined.

Drain current flows only for positive half-cycles of v_{sig} , as shown at left.

This is a periodic function, and therefore it has Fourier components:

$$i_D = a_0 + a_1 \sin \theta + a_2 \sin 2\theta + a_3 \sin 3\theta + \dots \quad (55)$$

The dc component a_0 can flow only through the choke:

$$I_{DC} = a_0 = \frac{1}{2\pi} \int_0^{2\pi} i_D d\theta = \frac{1}{2\pi} \int_0^{2\pi} I_p \sin \theta d\theta = \frac{I_p}{\pi} \quad (56)$$

Note that I_{DC} is simply the average value of i_D .

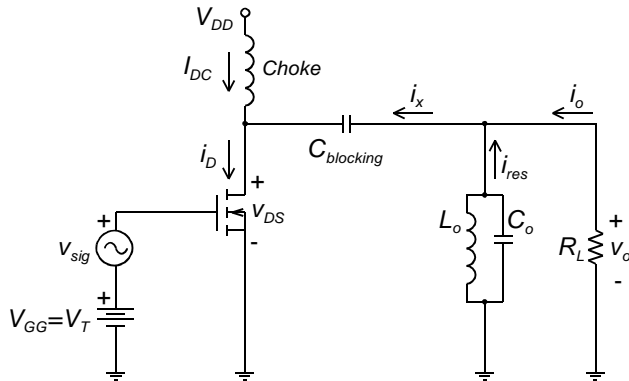


Fig. 35. Class B single-ended amplifier (Fig. 32 repeated).

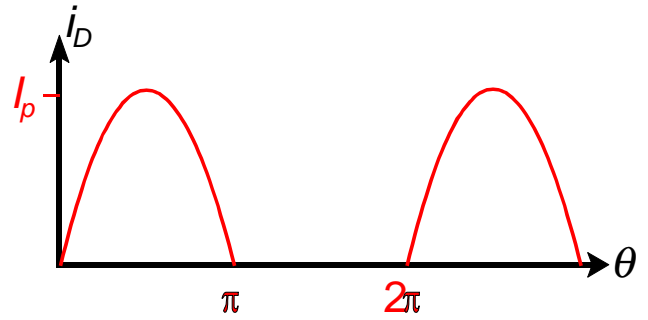


Fig. 36. Drain current in class B amplifier. (Fig. 34 repeated)

A KCL equation at the drain node gives:

$$i_D = I_{DC} + i_x \quad (57)$$

so we know that all of the sinusoidal components of i_D comprise i_x :

$$i_x = a_1 \sin \theta + a_2 \sin 2\theta + a_3 \sin 3\theta + \dots \quad (58)$$

Further, a KCL equation at the output node gives:

$$i_x = i_{res} + i_o \quad (59)$$

We know that the fundamental component at θ cannot flow through L_o - C_o , while the harmonic components at 2θ , 3θ , etc., can only flow through L_o - C_o . Thus:

$$i_o = a_1 \sin \theta \quad (60)$$

The magnitude a_1 of this fundamental component is found from a Fourier integral:

$$a_1 = \frac{1}{\pi} \int_0^{2\pi} i_D \sin \theta d\theta = \frac{1}{\pi} \int_0^{\pi} I_p \sin^2 \theta d\theta = \frac{I_p}{2} \quad (61)$$

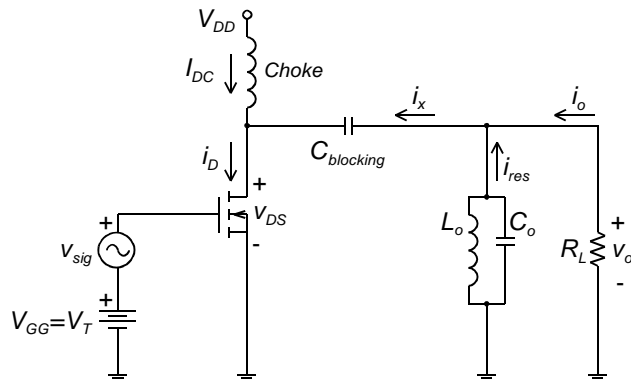


Fig. 37. Class B single-ended amplifier (Fig. 32 repeated).

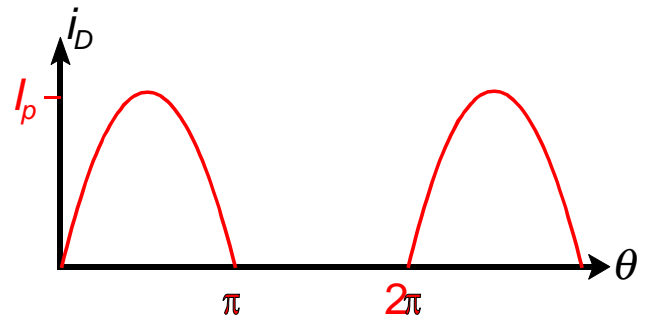


Fig. 38. Drain current in class B amplifier (Fig. 34 repeated).

The output voltage is produced by i_o flowing through R_L :

$$v_o = -\frac{I_p R_L}{2} \sin \theta = -V_m \sin \theta \quad (62)$$

which gives us the relationship between I_p and V_m :

$$I_p = \frac{2V_m}{R_L} \quad (63)$$

Now, we write a KVL equation around the drain-output loop:

$$V_{DS} = V_{C_{blocking}} + v_o = V_{DD} - V_m \sin \theta \quad (64)$$

and recognize that v_{DS} can't be negative, which limits the magnitude of v_o (before clipping of the output voltage occurs):

$$v_{DS} \geq 0 \quad \text{thus} \quad V_m \leq V_{DD} \quad (65)$$

It has taken us some effort (!!!), but we may finally proceed to the calculations.

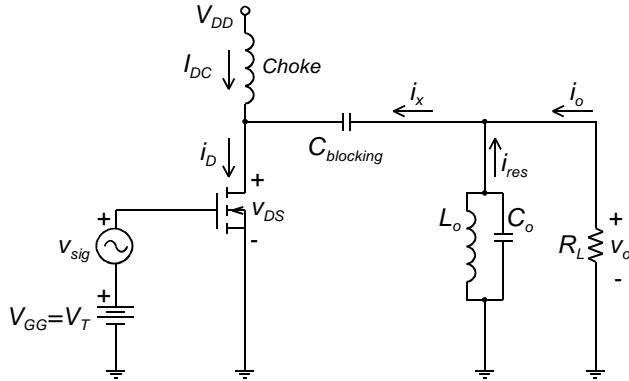


Fig. 39. Class B single-ended amplifier (Fig. 32 repeated).

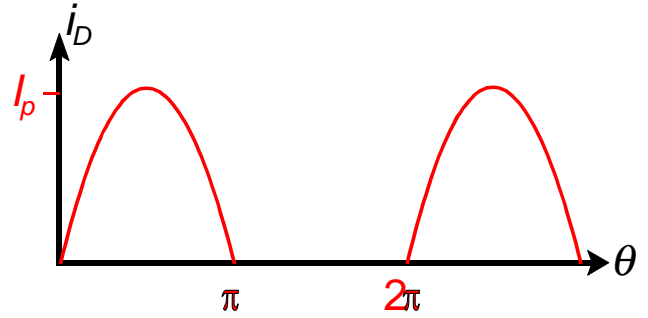


Fig. 40. Drain current in class B amplifier (Fig. 34 repeated).

Calculations:

1. Output Power

$$P_o = \frac{V_m^2}{2R_L} \quad \text{and} \quad P_{o_{\max}} = \frac{V_{DD}^2}{2R_L} \quad (66)$$

2. Input Power

$$P_{in} = V_{DD} I_{DC} = \frac{V_{DD} I_P}{\pi} = \frac{2V_{DD} V_m}{\pi R_L} \quad \text{and} \quad P_{in_{\max}} = \frac{2V_{DD}^2}{\pi R_L} \quad (67)$$

3. Efficiency

$$\eta = \frac{P_o}{P_{in}} = \frac{V_m^2 / 2R_L}{2V_{DD} V_m / \pi R_L} = \frac{\pi}{4} \left(\frac{V_m}{V_{DD}} \right) \quad \text{and} \quad \eta_{\max} = \frac{\pi}{4} = 78.5\% \quad (68)$$

4. Power Capability

$$C_P = \frac{P_{o_{\max}}}{v_{DS_{\max}} i_{D_{\max}}} = \frac{V_{DD}^2 / 2R_L}{(2V_{DD})(I_{p_{\max}})} = \frac{V_{DD}^2 / 2R_L}{(2V_{DD})(2V_{DD} / R_L)} = \frac{1}{8} \quad (69)$$

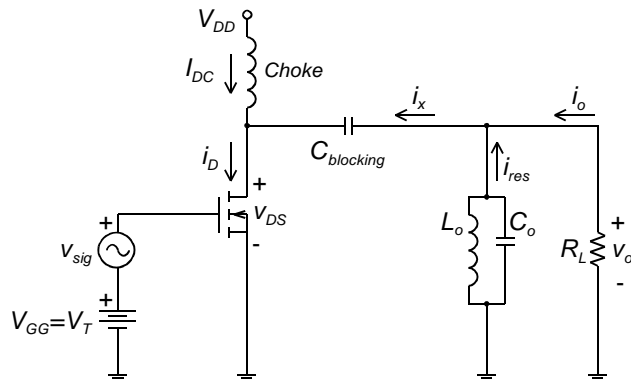


Fig. 41. Class B single-ended amplifier (Fig. 32 repeated).

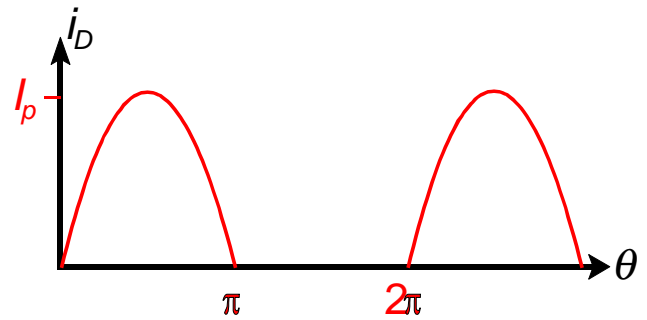


Fig. 42. Drain current in class B amplifier (Fig. 34 repeated).

5. FET Power Dissipation

$$P_Q = P_{in} - P_o = \frac{2V_{DD}V_m}{\pi R_L} - \frac{V_m^2}{2R_L} \quad (70)$$

To find $P_{Q_{max}}$ we need to set the derivative to zero:

$$\frac{\partial P_Q}{\partial V_m} = \frac{2V_{DD}}{\pi R_L} - \frac{V_m}{R_L} = 0 \quad (71)$$

from which

$$P_{Q_{max}} = \frac{4}{\pi^2} P_{o_{max}} = \frac{2V_{DD}^2}{\pi^2 R_L} \quad \text{at} \quad V_m = \frac{2V_{DD}}{\pi} \quad (72)$$

Notice that *all of these results are identical to those obtained earlier for the class B complementary amplifier!!!*

Introduction to Feedback

Feedback describes a technique used in amplifiers in which a fraction of the output signal is returned (fed back) to the input.

Negative Feedback

In negative feedback the returned portion subtracts from (opposes) the original input.

Benefits of negative feedback include:

- Stabilized gain (with variation of circuit parameters)
- Reduced nonlinear distortion
- Reduced noise (only some types of noise are reduced)
- Controlled Z_{in} and Z_{out}
- Increased bandwidth

The price we pay for these benefits, increased circuit complexity and reduced overall gain, are readily accepted given the capability of today's circuits.

Positive Feedback

In positive feedback the returned portion adds to (aids) the original input.

At one time (early 20th century) positive feedback was used to increase the gain over that obtainable with conventional circuits. The price was a degradation of all the items in the bulleted list, above.

No longer useful in amplifiers, it is required in oscillator circuits, Schmitt triggers, etc. We leave a discussion of positive feedback until later.

Closed-Loop Transfer Function

Consider the system represented by the block diagram, below. The negative sign at the summing block reflects our emphasis on negative feedback at this time.

If the path through the feedback network is opened, the gain from source to load is simply A , which is called the open-loop gain.

With the path through the feedback network closed, as shown, the gain changes to its closed-loop value.

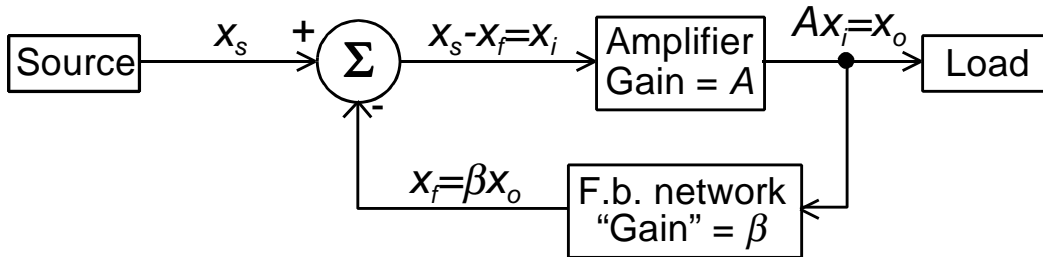


Fig. 43. Block diagram of generic feedback system. For electrical systems the variable x represents a voltage or a current.

Calculating the closed-loop gain is a matter of writing simple circuit equations for the above figure:

$$x_i = x_s - x_f = x_s - \beta x_o \quad (73)$$

$$x_o = Ax_i = A(x_s - \beta x_o) \quad (74)$$

$$x_o + A\beta x_o = Ax_s \quad (75)$$

$$\frac{x_o}{x_s} = A_f = \frac{A}{1 + A\beta} \quad (76)$$

A_f is called the closed-loop gain; the product $A\beta$ is the loop gain.

Repeating eq. (44):

$$\frac{x_o}{x_s} = A_f = \frac{A}{1 + A\beta} \quad (77)$$

Note that:

- For $A\beta > 0 \rightarrow A_f < A \rightarrow$ negative feedback
- For $A\beta < 0$ (and $|A\beta| < 1$) $\rightarrow A_f > A \rightarrow$ positive feedback
- If $A\beta = -1 \rightarrow$ oscillator
- In amplifiers, usually $A\beta \gg 1$ (A very large, β small). Thus:

$$A_f \approx \frac{1}{\beta} \quad (78)$$

Gain Stability

We can show that, for a typical negative feedback amplifier with $A\beta \gg 1$, the closed loop gain A_f is much more stable than the open-loop gain A . From eq. (77)

$$\frac{dA_f}{dA} = \frac{(1 + A\beta)(1) - (A)(\beta)}{(1 + A\beta)^2} = \frac{1}{(1 + A\beta)^2} \quad (79)$$

$$dA_f = dA \frac{1}{(1 + A\beta)^2} = \frac{dA}{A} \frac{A}{(1 + A\beta)^2} = \frac{dA}{A} \frac{A_f}{1 + A\beta} \quad (80)$$

$$\frac{dA_f}{A_f} = \frac{dA}{A} \frac{1}{1 + A\beta} \quad (81)$$

Thus, an incremental change in A results in a much smaller change in A_f .

Reduction of Nonlinear Distortion

It is relatively easy to produce a small-signal amplifier that is reasonably linear. It is much more difficult to produce a linear power amplifier. Suppose we have a power amplifier with a nonlinear characteristic. The output would be very distorted, as shown below for an assumed sinusoidal input:

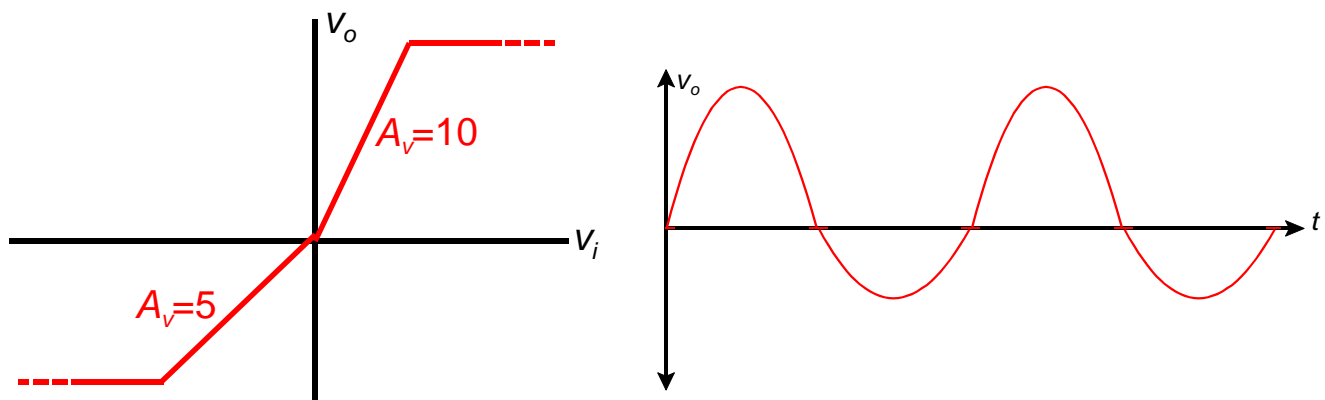


Fig. 44. Amplifier with exaggerated nonlinear characteristic.

Fig. 45. Nonlinear amplifier output.

But if we embed this amplifier in a feedback system with a linear high-gain preamplifier:

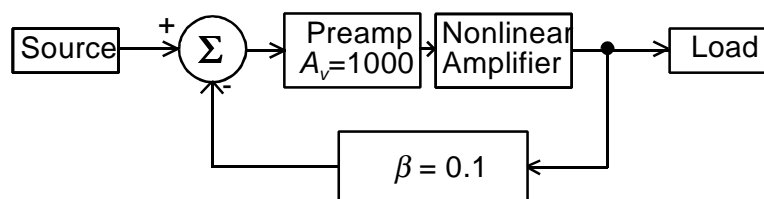


Fig. 46. Improving overall linearity with negative feedback.

For positive v_i , $A = (1000)(10) = 10,000$, $A_f = A / (1 + \beta A) = 9.99$

For negative v_i , $A = (1000)(5) = 5,000$, $A_f = A / (1 + \beta A) = 9.98$

Note that the closed-loop gain is very nearly linear!!!

Reduction of Noise

If we can construct a single low-noise amplifier stage, we can reduce considerably the overall noise in an amplifier system.

Noise Sources:

Johnson noise - thermally generated in resistors.

Shot noise - due to discrete nature of current flow.

Microphonic noise - due to vibration of components.

Miscellaneous noise - power supply hum, stray coupling.

Noise Models:

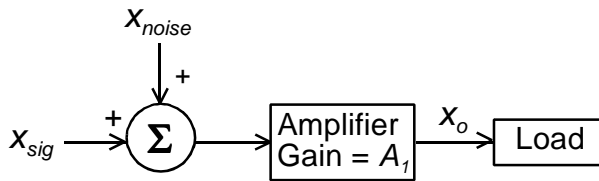


Fig. 47. Noise referred to input.

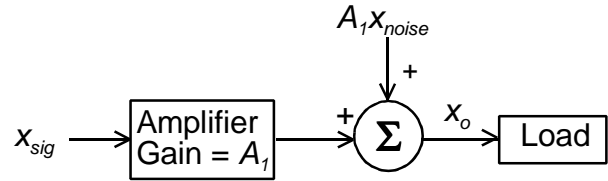


Fig. 48. Noise referred to output.

Signal-to-Noise Ratio, SNR:

$$SNR = \frac{P_{signal}}{P_{noise}} = \frac{\text{signal power delivered to load}}{\text{noise power delivered to load}} \quad (82)$$

where:

$$P_{signal} = \frac{(A_1 x_{sig})^2}{R_L} \quad \text{and} \quad P_{noise} = \frac{(A_1 x_{noise})^2}{R_L} \quad (83)$$

Thus:

$$SNR = \frac{x_{sig}^2}{x_{noise}^2} \quad (84)$$

Signal-to-Noise Ratio is usually expressed in decibels:

$$SNR_{dB} = 10 \log SNR = 10 \log \frac{P_{signal}}{P_{noise}} = 20 \log \frac{X_{sig}}{X_{noise}} \quad (85)$$

Reduction of Noise Using Feedback:

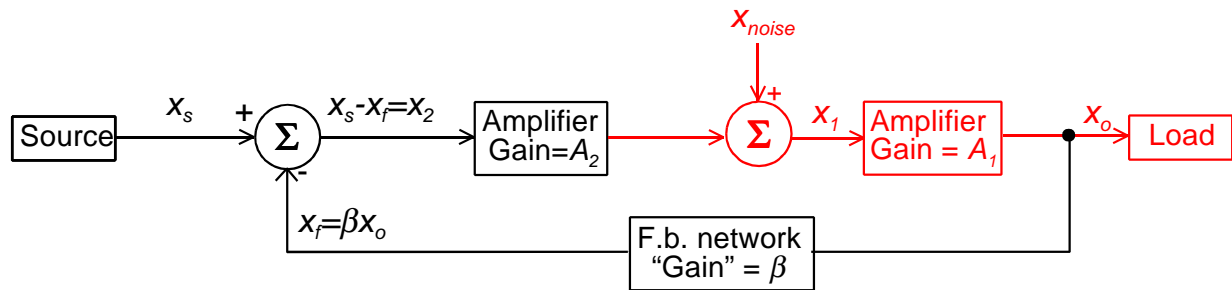


Fig. 49. The noise model of Fig. 47 embedded in an otherwise noiseless feedback network.

Beginning at the output and working backwards gives the equation:

$$x_o = A_1 x_1 = A_1 (A_2 x_2 + x_{noise}) = A_1 [A_2 (x_s - \beta x_o) + x_{noise}] \quad (86)$$

Now, solving eq. (86) for x_o :

$$(1 + A_1 A_2 \beta) x_o = A_1 A_2 x_s + A_1 x_{noise} \quad (87)$$

$$x_o = x_s \frac{A_1 A_2}{1 + A_1 A_2 \beta} + x_{noise} \frac{A_1}{1 + A_1 A_2 \beta} \quad (88)$$

The signal-to-noise ratio is greatly improved (by A_2^2):

$$SNR = \frac{(1^{st} \text{ term})^2}{(2^{nd} \text{ term})^2} = \frac{x_s^2}{x_{noise}^2} A_2^2 \quad (89)$$

Types of Feedback

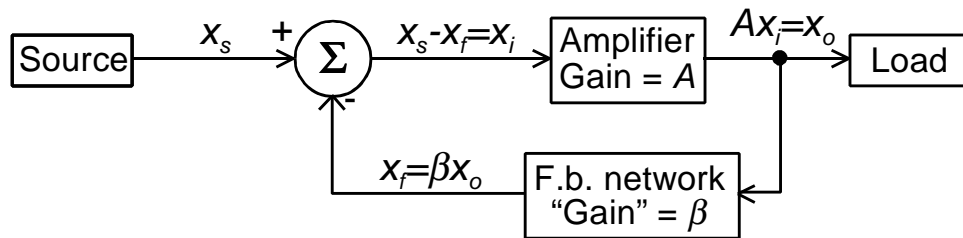


Fig. 50. Block diagram of generic feedback system. For electrical systems the variable x represents a voltage or a current (Fig. 43 repeated).

As described in the figure above, either voltage or current can be “sampled” (measured) at the output, and either voltage or current can be fed back to the summing block. Thus, there are four possible feedback configurations. The descriptions follow the form input - output.

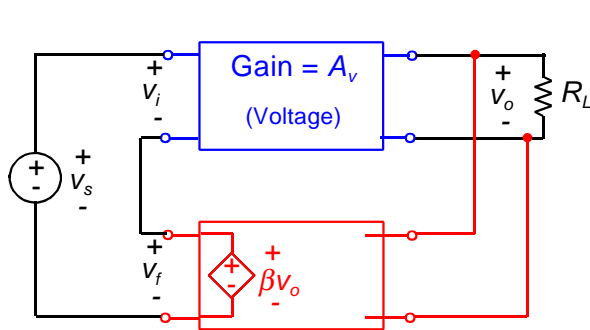


Fig. 51. Series-voltage feedback.

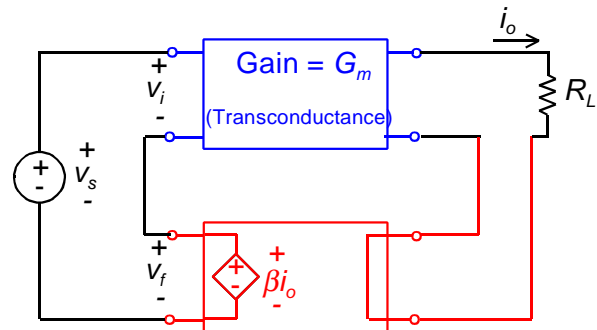


Fig. 52. Series-current feedback.

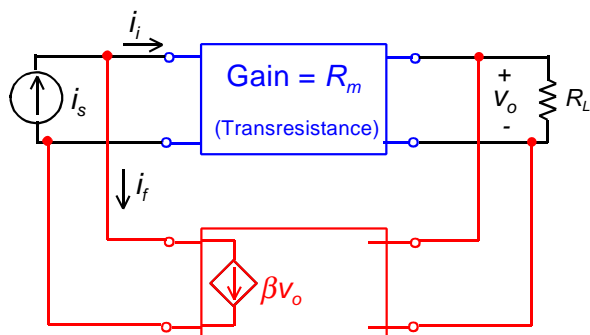


Fig. 53. Parallel-voltage feedback.

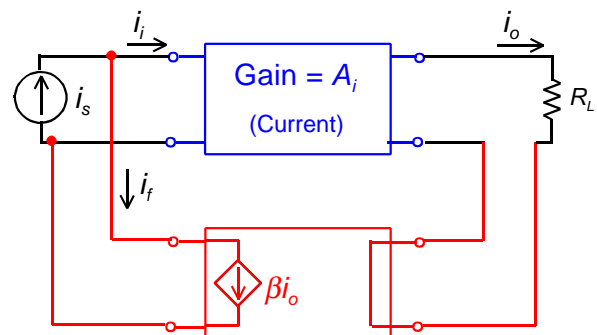


Fig. 54. Parallel-current feedback.

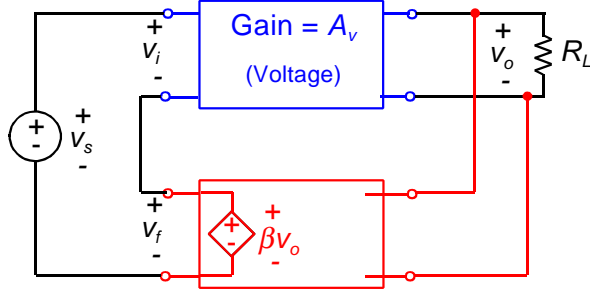


Fig. 55. Series-voltage feedback.

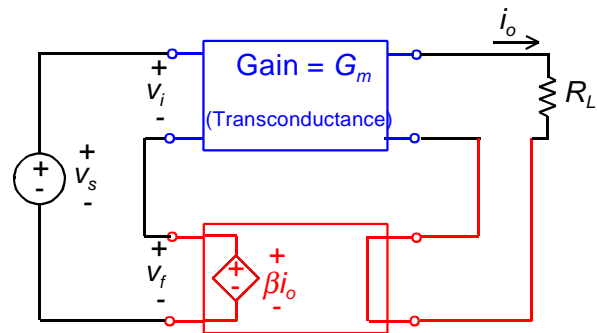


Fig. 56. Series-current feedback.

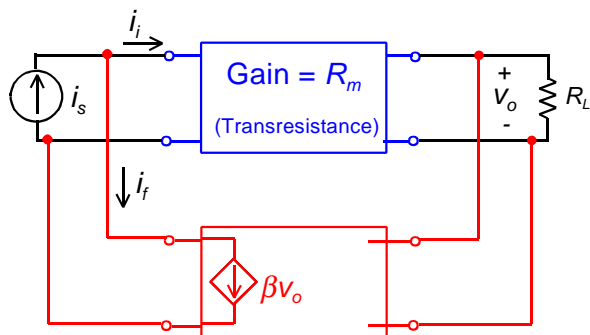


Fig. 57. Parallel-voltage feedback.

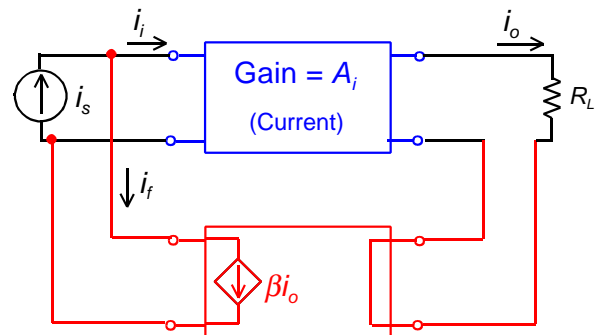


Fig. 58. Parallel-current feedback.

On the Input Side

We use the term series-mixing with voltages, because voltages add or subtract in series, and we model the signal as a voltage source.

We use the term parallel-mixing (or shunt-mixing) with currents, because currents add or subtract in parallel, and we model the signal as a current source.

On the Output Side

We use the term voltage-sensing when voltage is the sampled output variable, which must be done with a parallel connection.

We use the term current-sensing when current is the sampled output variable, which must be done with a series connection.

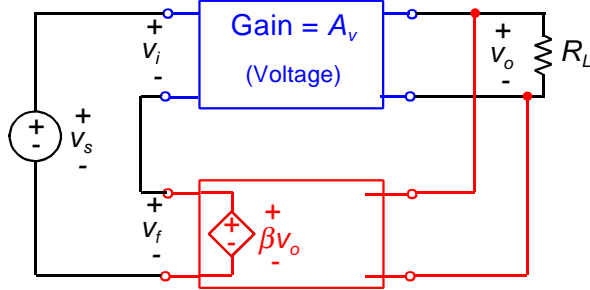


Fig. 59. Series-voltage feedback.

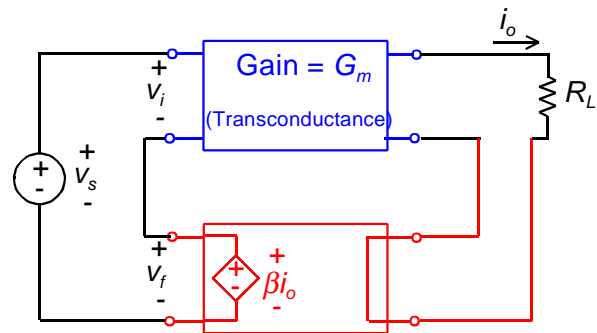


Fig. 60. Series-current feedback.

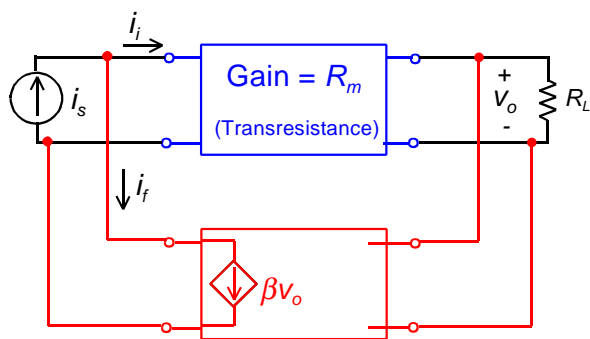


Fig. 61. Parallel-voltage feedback.

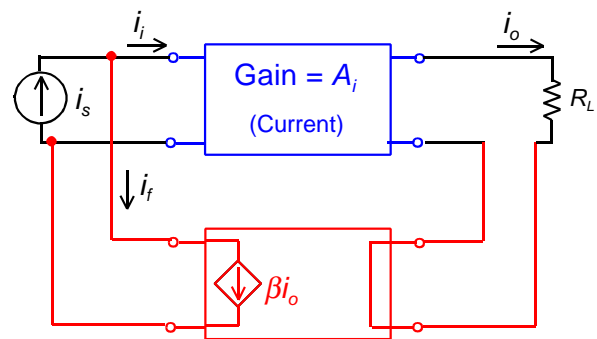


Fig. 62. Parallel-current feedback.

The Amplifier Block

Any *real* amplifier can be modeled as voltage, current, transconductance, or transresistance.

We (naturally) choose the model appropriate for the type of feedback connection.

The Feedback Block

Units of the feedback factor β are the inverse of the units of open-loop gain A , i.e., the loop gain $A\beta$ is always unitless!!!

In our models the feedback network is assumed to be ideal, i.e., either an ideal voltage or current source at the input, and either a short-circuit or open-circuit at the load.

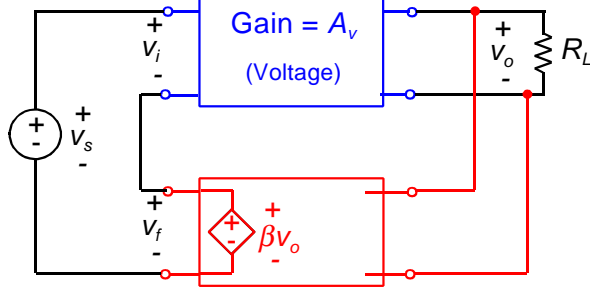


Fig. 63. Series-voltage feedback.

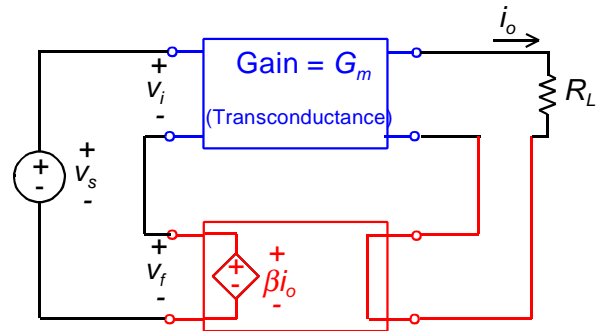


Fig. 64. Series-current feedback.

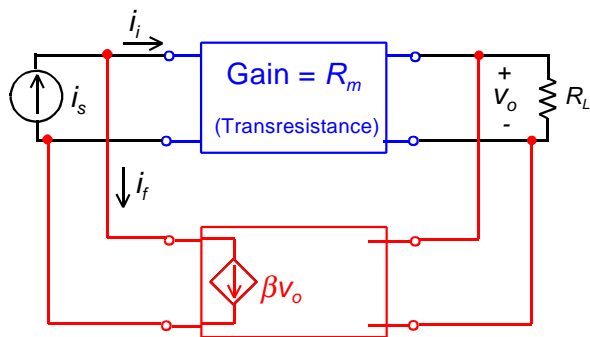


Fig. 65. Parallel-voltage feedback.

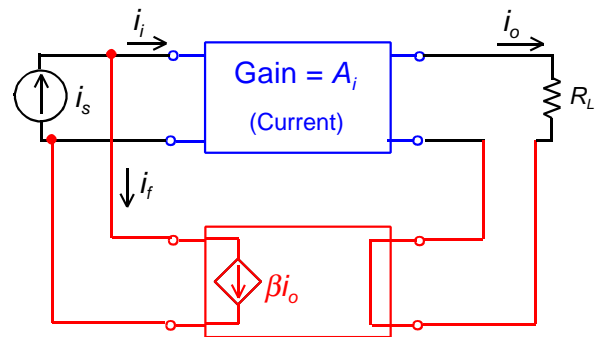


Fig. 66. Parallel-current feedback.

Gain Equations

The form of our generic gain equation (44) can be changed to more appropriately reflect the type of feedback:

<p>Series-voltage:</p> $A_{v_f} = \frac{V_o}{V_s} = \frac{A_v}{1 + A_v \beta} \quad (90)$ <p>stabilized voltage gain</p>	<p>Series-current:</p> $G_{m_f} = \frac{i_o}{V_s} = \frac{G_m}{1 + G_m \beta} \quad (91)$ <p>stabilized transconductance gain</p>
<p>Parallel-voltage:</p> $R_{m_f} = \frac{V_o}{i_s} = \frac{R_m}{1 + R_m \beta} \quad (92)$ <p>stabilized transresistance gain</p>	<p>Parallel-current:</p> $A_{i_f} = \frac{i_o}{i_s} = \frac{A_i}{1 + A_i \beta} \quad (93)$ <p>stabilized current gain</p>

Effect on Input Resistance

The type of feedback effects the input resistance of the system, as we see in the following pages.

Series Mixing:

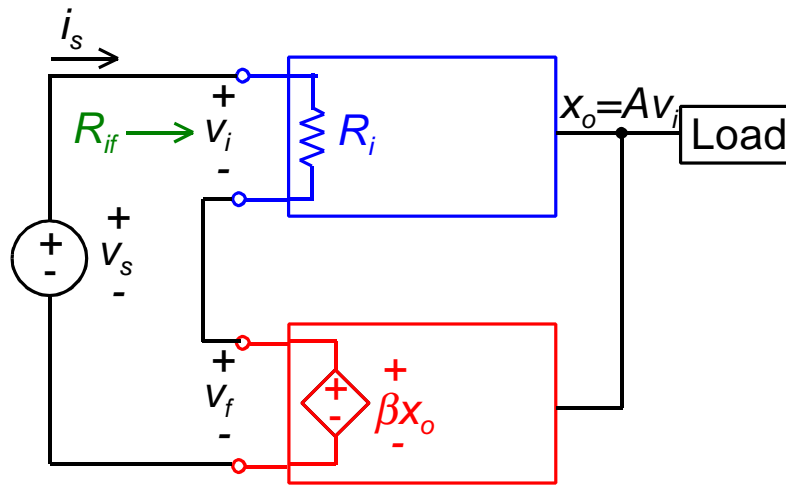


Fig. 67. Feedback system with series-mixing input and generic output.

The input resistance of the amplifier is R_i , though the signal source sees an input resistance of R_{if} .

From KVL:

$$\begin{aligned}
 V_s &= V_i + V_f \\
 &= i_s R_i + \beta x_o = i_s R_i + \beta (A V_i) = i_s R_i + \beta (A i_s R_i) \\
 &= (1 + A\beta) i_s R_i
 \end{aligned} \tag{94}$$

Thus,

$$R_{if} = \frac{V_s}{i_s} = \frac{(1 + A\beta) i_s R_i}{i_s} = (1 + A\beta) R_i \tag{95}$$

Series-mixing increases input resistance!!!

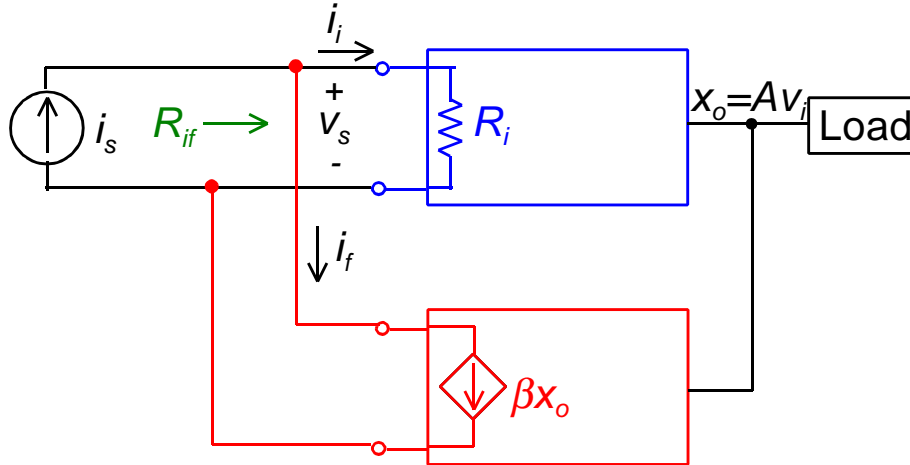
Parallel Mixing:

Fig. 68. Feedback system with parallel-mixing input and generic output.

As in the previous example, the input resistance of the amplifier is R_i , though the signal source sees an input resistance of R_{if} .

From KCL:

$$\begin{aligned}
 i_s &= i_i + i_f \\
 &= \frac{V_s}{R_i} + \beta x_o = \frac{V_s}{R_i} + \beta (Av_i) = \frac{V_s}{R_i} + \beta \left(A \frac{V_s}{R_i} \right) \\
 &= (1 + A\beta) \frac{V_s}{R_i}
 \end{aligned} \tag{96}$$

Thus,

$$R_{if} = \frac{V_s}{i_s} = \frac{V_s}{(1 + A\beta) \frac{V_s}{R_i}} = \frac{R_i}{1 + A\beta} \tag{97}$$

Parallel-mixing decreases input resistance!!!

Effect on Output Resistance

The type of feedback also effects the output resistance of the system, as we see in the following pages.

Voltage Sensing:

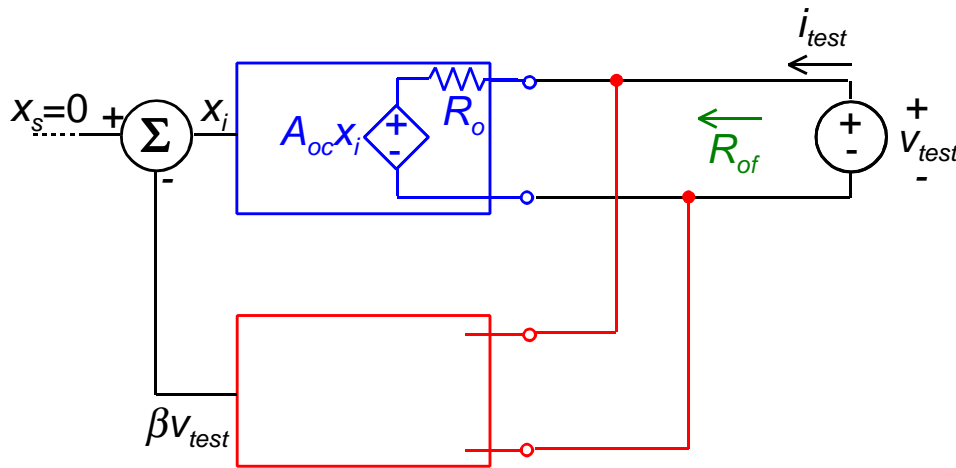


Fig. 69. Feedback system with generic input and voltage sensing at the output.

The output resistance of the amplifier is R_o , though the load (or test source) sees an output resistance of R_{of} .

From KCL:

$$\begin{aligned} v_{test} &= i_{test} R_o + A_{oc} x_i \\ &= i_{test} R_o + A_{oc} (-\beta v_{test}) \end{aligned} \quad (98)$$

Rearranging:

$$(1 + A_{oc} \beta) v_{test} = i_{test} R_o \quad (99)$$

Thus:

$$R_{of} = \frac{v_{test}}{i_{test}} = \frac{R_o}{1 + A_{oc} \beta} \quad (100)$$

Voltage sensing decreases output resistance!!!

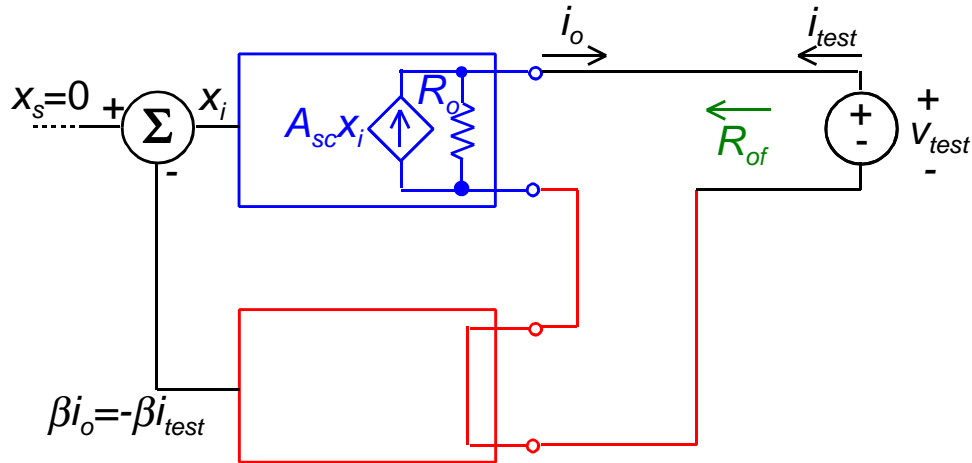
Current Sensing:

Fig. 70. Feedback system with generic input and current sensing at the output.

As in the previous example, the output resistance of the amplifier is R_o , though the load (or test source) sees an output resistance of R_{of} .

From KCL:

$$i_{test} = \frac{V_{test}}{R_o} - A_{sc} x_i = \frac{V_{test}}{R_o} - A_{sc} (\beta i_{test}) \quad (101)$$

Rearranging:

$$(1 + A_{sc} \beta) i_{test} = \frac{V_{test}}{R_o} \quad (102)$$

Thus:

$$R_{of} = \frac{V_{test}}{i_{test}} = (1 + A_{sc} \beta) R_o \quad (103)$$

Current sensing increases output resistance!!!

Summary of Feedback Types

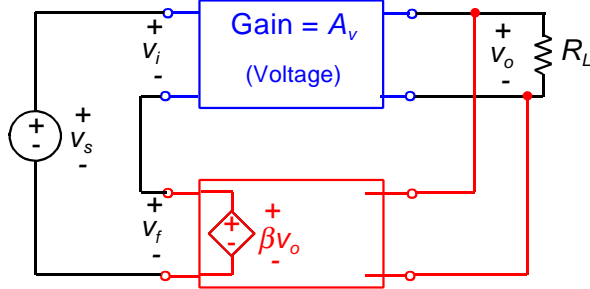


Fig. 71. Series-voltage feedback.

Input: voltage source
Output variable: voltage

R_{if} and R_{of} tend toward: Ideal
Voltage Amplifier

$$A_{v_f} = \frac{A_v}{1 + A_v \beta}$$

$$R_{i_f} = (1 + A_v \beta) R_i$$

$$R_{o_f} = \frac{R_o}{1 + A_{v_{oc}} \beta}$$

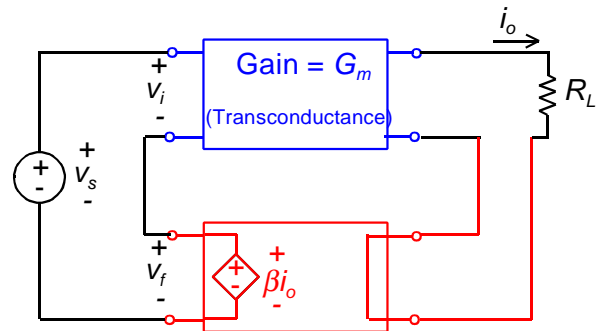


Fig. 72. Series-current feedback.

Input: voltage source
Output variable: current

R_{if} and R_{of} tend toward: Ideal
Transconductance Amplifier

$$G_{m_f} = \frac{G_m}{1 + G_m \beta}$$

$$R_{i_f} = (1 + G_m \beta) R_i$$

$$R_{o_f} = (1 + G_{m_{sc}} \beta) R_o$$

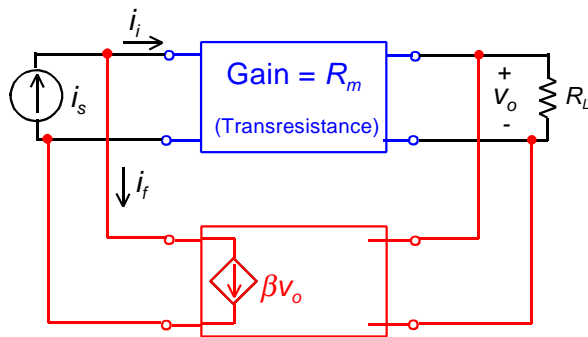


Fig. 73. Parallel-voltage feedback.

Input: current source
Output variable: voltage

R_{if} and R_{of} tend toward: Ideal
Transresistance Amplifier

$$R_{m_f} = \frac{R_m}{1 + R_m \beta}$$

$$R_{i_f} = \frac{R_i}{1 + R_m \beta}$$

$$R_{o_f} = \frac{R_o}{1 + R_{m_{oc}} \beta}$$

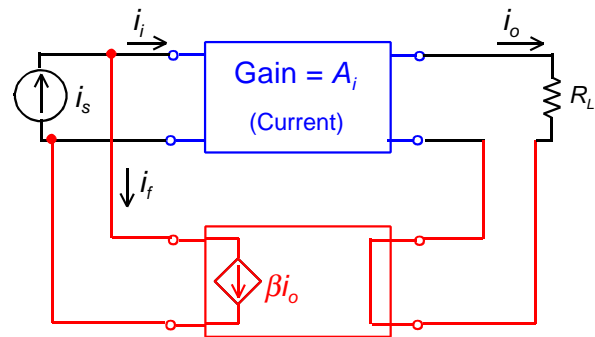


Fig. 74. Parallel-current feedback.

Input: current source
Output variable: current

R_{if} and R_{of} tend toward: Ideal
Current Amplifier

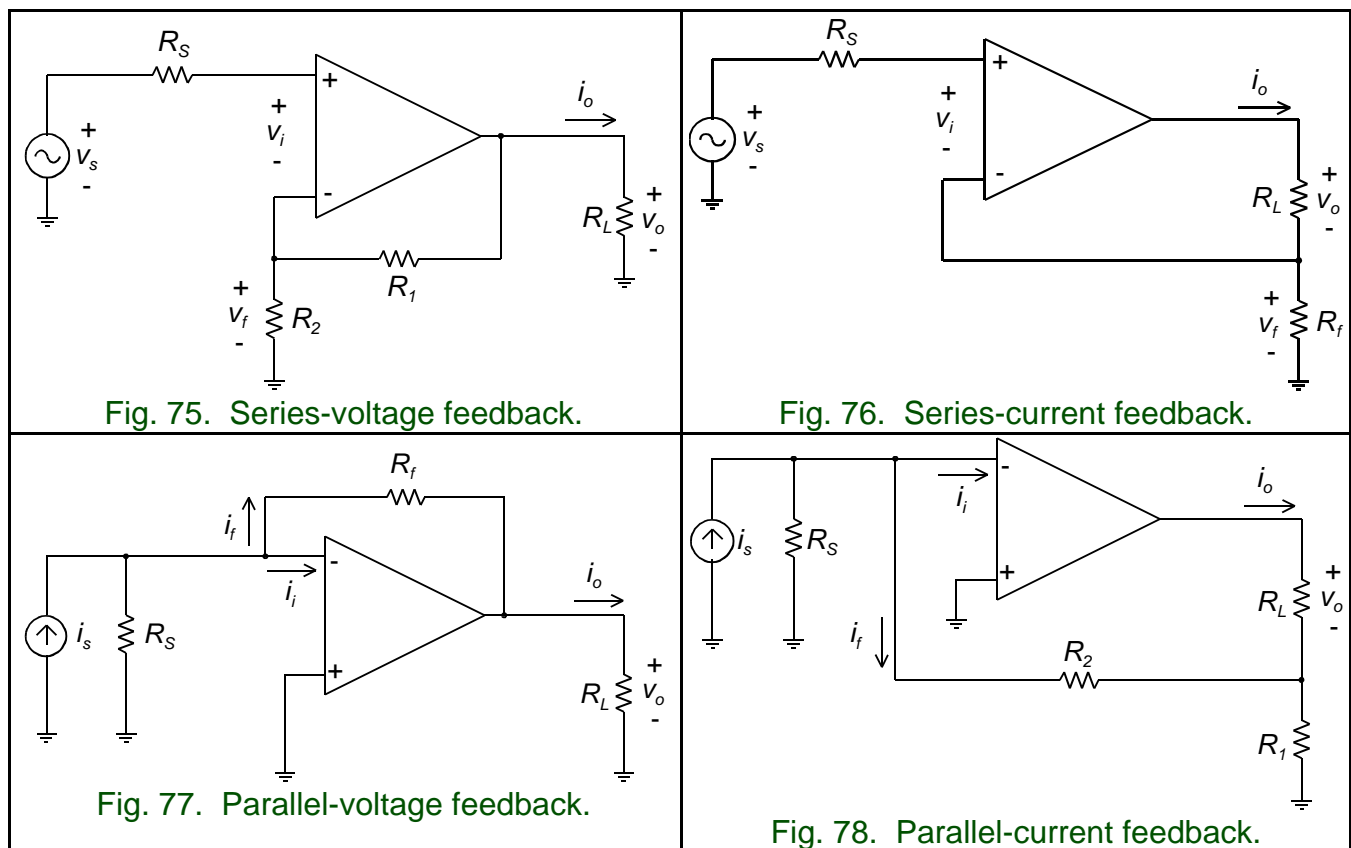
$$A_{i_f} = \frac{A_i}{1 + A_i \beta}$$

$$R_{i_f} = \frac{R_i}{1 + A_i \beta}$$

$$R_{o_f} = (1 + A_{i_{sc}} \beta) R_o$$

Practical Feedback Networks

It's impossible, of course, to show all possible practical feedback networks. The four shown below are very typical examples:



Identifying Feedback Configuration

At the Input:

Look for series or parallel connection. Remember that the signal source, the amplifier input port, and the feedback network output port each have two terminals.

At the Output:

Look for series or parallel connection here, also. Alternatively, if a short-circuited load causes x_f to be zero, the connection is voltage sensing. Conversely, if an open-circuited load causes x_f to be zero, the connection is current sensing.

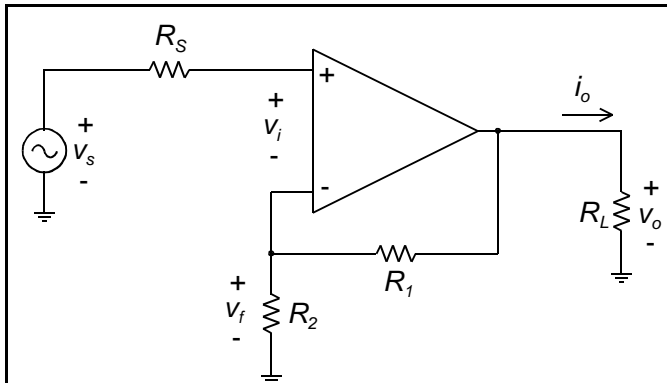


Fig. 79. Series-voltage feedback.

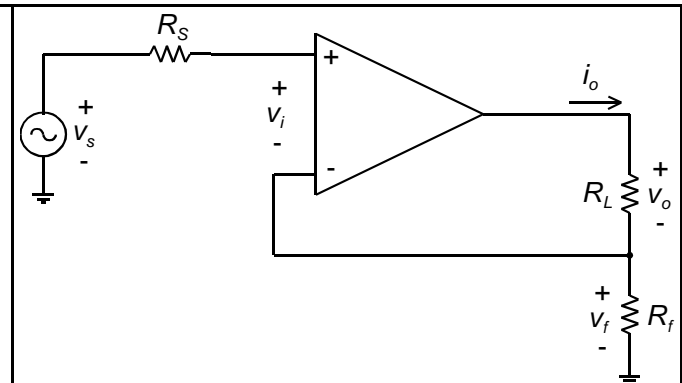


Fig. 80. Series-current feedback.

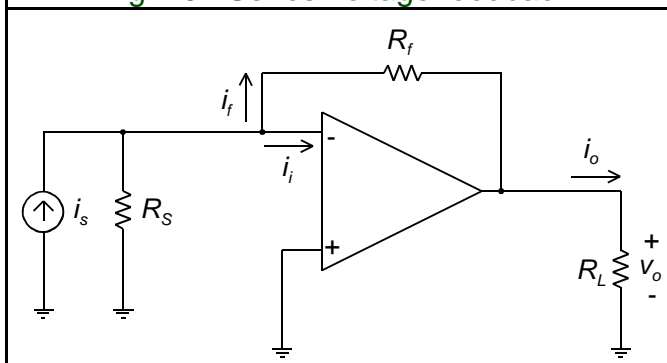


Fig. 81. Parallel-voltage feedback.

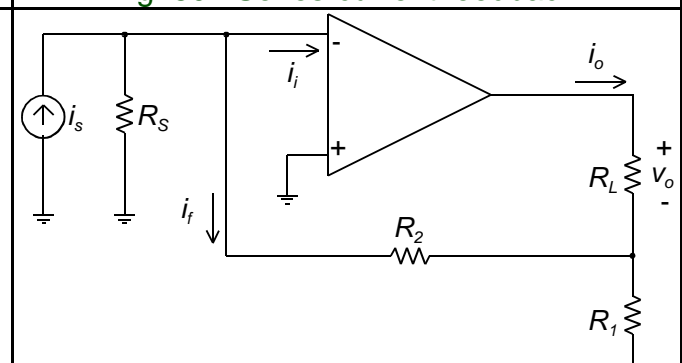


Fig. 82. Parallel-current feedback.

Identifying Negative Feedback

The feedback is negative if:

- a change in x_s that tends to *increase* x_i . . .
- causes a change in x_f that tends to *decrease* x_i .

Estimating the Feedback Factor

We estimate the feedback factor, β , by idealizing the circuit. Note that the amplifier input acts as a *load* to the feedback network.

To estimate β , we assume the amplifier input is ideal, i.e.:

- an open-circuit for series mixing,
- a short-circuit for parallel mixing.

Design of Feedback Amplifiers

1. Determine type of feedback and value of β required.
 2. Choose appropriate feedback network (basic versions in Figs. 75 - 78).
 3. Choose appropriate resistor values
 - (a) β often dependent only on ratio of resistors.
 - (b) Real feedback networks have nonideal input and output resistances - they are not the ideal-dependent-source models of Figs. 71 - 74.
 - (c) These real feedback networks load the amplifier output and insert unwanted resistance into the amplifier input.
 - (d) To minimize loading effects (must often compromise):
 - (i) Series Mixing - small R's to minimize series voltage drop
 - (ii) Parallel Mixing - large R's to minimize load on signal source
 - (iii) Voltage Sensing - large R's to minimize load on amplifier output
 - (iv) Current Sensing - small R's to minimize series voltage drop
 4. Analyze/simulate/test to insure design specifications are met.
-

Transient and Frequency Response in Feedback Amplifiers

Introduction

As a practical matter, in feedback systems both the gain, A , and the feedback factor, β , are functions of frequency:

$$A_f(s) = \frac{A(s)}{1 + A(s)\beta(s)} \quad (104)$$

Recall:

- Zeros are those values of s for which $A_f(s) = 0$.
- Poles are those values of s for which $A_f(s) = \infty$, i.e., the roots of $1 + A(s)\beta(s) = 0$.
- Poles and zeros may be complex (real σ ; imaginary $j\omega$).
- Poles and zeros of a transfer function may be illustrated graphically on the complex plane (the s -plane).
- For physically realizable circuits, complex poles always occur in conjugate pairs.

Transient Response

Transfer function poles lead to transient response terms of the form:

$$e^{st} = e^{(\sigma + j\omega)t} = e^{\sigma t} (A \cos \omega t + jB \sin \omega t) \quad (105)$$

Transient Response and Pole Location

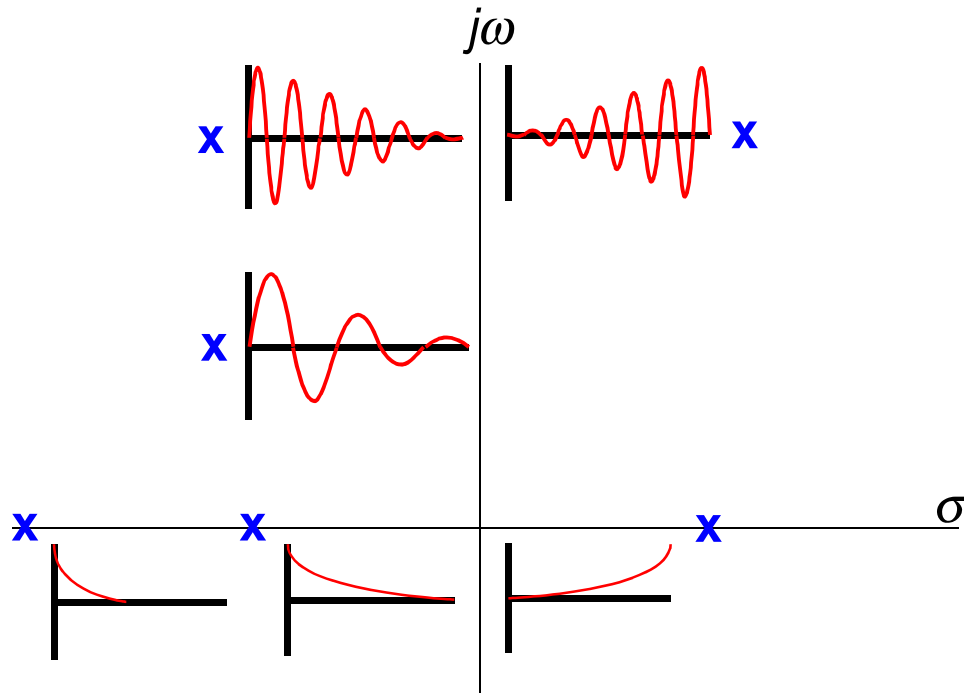


Fig. 83. Illustration of various transient responses with s-plane pole locations.

For poles on the negative real axis, the transient response has the form $e^{-\sigma t}$, where $1/\sigma = \tau$.

For poles on the positive real axis, the transient response has the form $e^{\sigma t}$.

For complex conjugate poles at $s = \sigma \pm j\omega$

- Transient response form: $e^{\sigma t} (A \cos \omega t + jB \sin \omega t)$
- Transfer function form: $(s + \sigma + j\omega)(s + \sigma - j\omega) = s^2 + 2\delta\omega_n s + \omega_n^2$
- Natural frequency $\omega_n = \sqrt{\sigma^2 + \omega^2}$
- Damping ratio $\delta = \sigma/\omega_n$ (Quality factor, $Q = 1/2\delta$)

Frequency Response and Pole Location

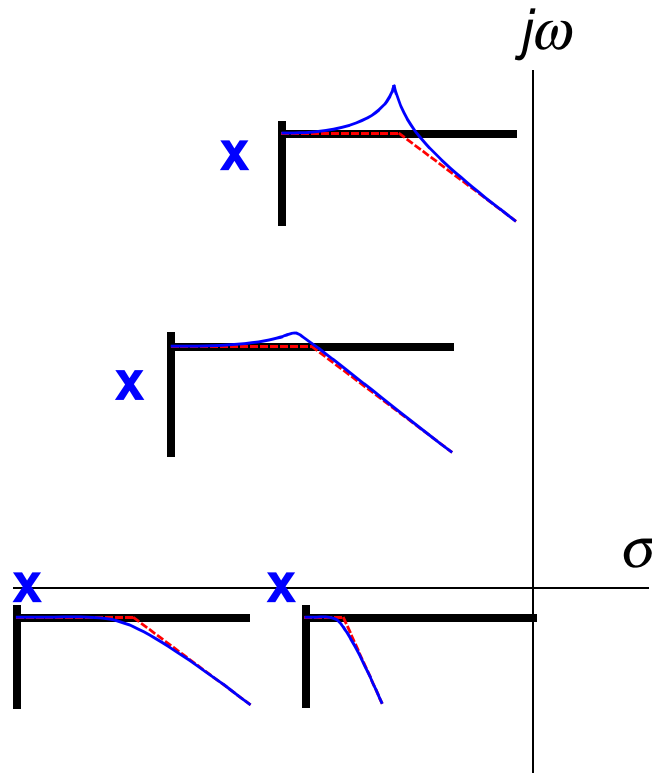


Fig. 84. Illustration of various frequency (magnitude) responses with s-plane pole locations.

Bode Plots use poles and zeros to determine the asymptotes of the magnitude and phase responses. The Bode asymptotes are shown above in red.

As the poles move off of the negative real axis, the asymptotes do not change, but the actual magnitude response exhibits gain peaks.

These gain peaks increase as the poles approach the $j\omega$ axis.

Graphical Details of Complex Conjugate Poles

These are graphical details, so let's let the figures tell the story:

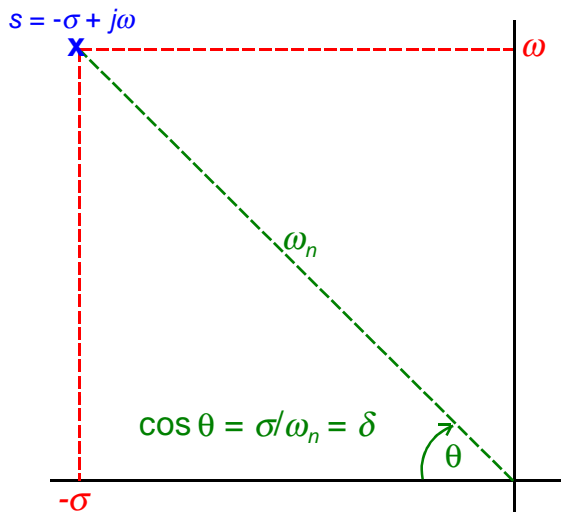


Fig. 85. One of two complex conjugate poles showing the relationship among transfer function parameters

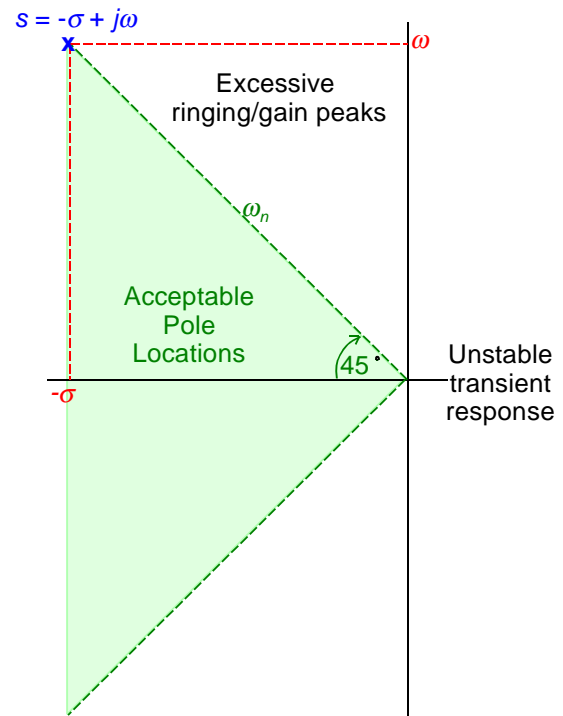


Fig. 86. Illustration of acceptable pole locations using 45° "rule of thumb."

In amplifiers we normally choose, somewhat arbitrarily, a region of pole locations where transient response ringing and frequency response gain peaks are considered to be within acceptable limits.

The typical rule of thumb allows poles to be located within a 45° angles from the negative real axis.

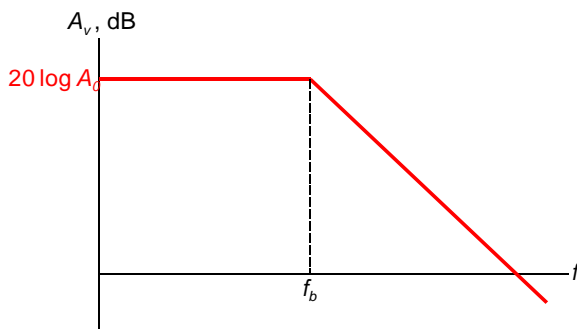
Note that the 45° rule of thumb illustrated in Fig. 86 requires $\sigma \geq \omega$ (which means $\delta \geq 0.707$ and $Q \leq 0.707$) for acceptable stability.

Frequency Characteristics of Feedback Amplifiers

Dominant-Pole Amplifiers

A dominant-pole amplifier may have many poles, but one pole is much lower in frequency than the others, and dominates the responses as if there were only one pole.

All real amplifiers have one or more zeros at $s = \infty$. In this sense they are lowpass. So consider a single-pole (dominant-pole) lowpass amplifier:



$$A(s) = \frac{A_0}{\frac{s}{2\pi f_b} + 1} \quad (106)$$

Fig. 87. Single-pole lowpass Bode magnitude response.

Now let's add negative feedback to this amplifier using a purely resistive, and thus frequency independent, feedback network:

$$\begin{aligned} A_f(s) &= \frac{A(s)}{1 + A(s)\beta} = \frac{A_0}{\frac{s}{\omega_b} + 1} \cdot \frac{1}{1 + \frac{A_0\beta}{\frac{s}{\omega_b} + 1}} \\ &= \frac{A_0}{\frac{s}{\omega_b} + 1} \cdot \frac{1}{\frac{s}{\omega_b} + 1 + A_0\beta} = \frac{A_0}{\frac{s}{\omega_b} + 1 + A_0\beta} \end{aligned} \quad (107)$$

Continuing with eq.(107) and solving:

$$A_f(s) = \frac{A_0}{\frac{s}{\omega_b} + 1 + A_0\beta} = \frac{\frac{A_0}{1 + A_0\beta}}{\frac{s}{\omega_b(1 + A_0\beta)} + 1} = \frac{A_{0_f}}{\frac{s}{2\pi f_{b_f}} + 1} \quad (108)$$

where

$$A_{0_f} = \frac{A_0}{1 + A_0\beta} \quad \text{and} \quad f_{b_f} = f_b(1 + A_0\beta) \quad (109)$$

Thus, the feedback amplifier also has a single-pole lowpass response, but:

1. DC gain is reduced by the factor $(1 + A_0\beta)$ as usual.
2. Bandwidth is increased by a factor of $(1 + A_0\beta)$!!!

Gain-Bandwidth Product:

The notation GB or GBW is normally used to denote this measure. We obtain it by noting that:

$$A_{0_f} f_{b_f} = \frac{A_0}{1 + A_0\beta} \bullet f_b(1 + A_0\beta) = A_0 f_b \quad (110)$$

i.e.,

$$GBW = A_{0_f} f_{b_f} = A_0 f_b \quad (111)$$

This latter equation says that the gain-bandwidth product of a feedback system using a dominant pole amplifier is independent of the amount of feedback, β , applied!!!

It is also equal to the GBW of the original dominant-pole amplifier!!!

Dominant-Pole Gain-Bandwidth Example:

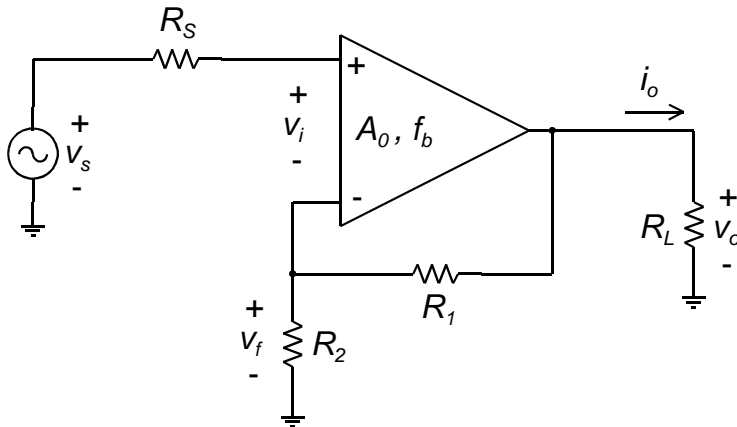


Fig. 88. Dominant-pole example.

An operational amplifier has a dominant (single) pole response with:

$$A_o = 10^5 \rightarrow 100 \text{ dB}$$

$$f_b = 10 \text{ Hz}$$

Feedback factors to be used with this amplifier are $\beta = 0.01, 0.1$, and 1

β	$A_{of} = A_o / (1 + A_o \beta)$	$A_{of} \approx 1/\beta$	$f_{bf} = f_b (1 + A_o \beta)$
0.01	99.90	100	10.01 kHz
0.1	9.999	10	100.0 kHz
1	1.000	1	1.000 MHz

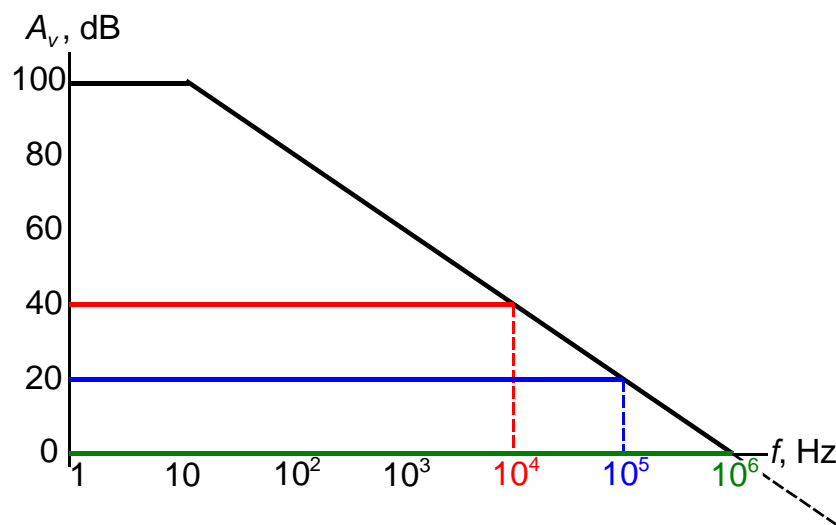


Fig. 89. Bode plots showing constant GBW.

Feedback Factor and Pole Location:

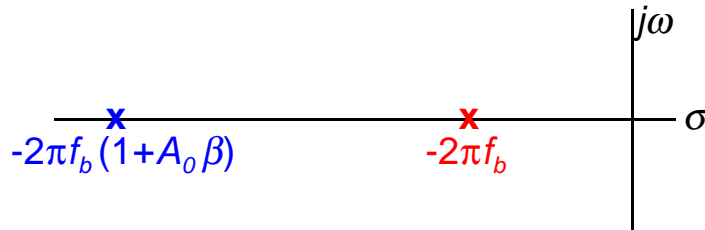


Fig. 90. Movement of the dominant pole with feedback.

The pole moves to the left with feedback, as shown.

From the form of the transient response, $e^{-\sigma t}$, we can see that the response decays faster as pole moves left.

Summary:

- Many multiple-pole amplifiers have a dominant pole, i.e., a pole much closer to the origin than all other poles.
- The dominant pole transient response lasts much longer than the transient response of the other poles.
- A dominant-pole amplifier may be treated like a single-pole amplifier (usually).
- Dominant-pole amplifiers have a constant gain-bandwidth product.

Two-Pole Amplifiers

Let's presume we have a two-pole amplifier with both poles on the negative real axis:

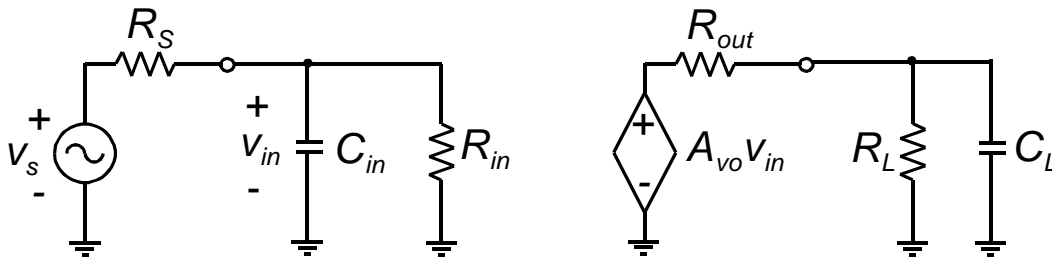


Fig. 91. Model of amplifier with two lowpass poles

$$A(s) = \frac{A_0}{\left(\frac{s}{2\pi f_1} + 1 \right) \left(\frac{s}{2\pi f_2} + 1 \right)} \quad (112)$$

Now let's add negative feedback to this amplifier using a purely resistive (thus frequency independent) feedback network:

$$A_f(s) = \frac{A(s)}{1 + A(s)\beta} \quad (113)$$

The *closed-loop poles* (the poles of the resulting feedback amplifier) are given by the roots of $1 + A(s)\beta$:

$$\begin{aligned} 1 + A(s)\beta &= 1 + \frac{A_0\beta}{\left(\frac{s}{\omega_1} + 1 \right) \left(\frac{s}{\omega_2} + 1 \right)} \\ &= 1 + \frac{A_0\beta}{\frac{s^2}{\omega_1\omega_2} + \frac{s}{\omega_1} + \frac{s}{\omega_2} + 1} \end{aligned} \quad (114)$$

Setting eq. (114) to zero and continuing to work the right-hand side:

$$\begin{aligned}
 0 &= 1 + \frac{A_0 \beta \omega_1 \omega_2}{s^2 + s(\omega_1 + \omega_2) + \omega_1 \omega_2} \\
 &= \frac{s^2 + s(\omega_1 + \omega_2) + \omega_1 \omega_2}{s^2 + s(\omega_1 + \omega_2) + \omega_1 \omega_2} + \frac{A_0 \beta \omega_1 \omega_2}{s^2 + s(\omega_1 + \omega_2) + \omega_1 \omega_2}
 \end{aligned} \tag{115}$$

Now we have a common denominator, thus, the sum of the numerators must equal zero:

$$s^2 + s(\omega_1 + \omega_2) + (1 + A_0 \beta) \omega_1 \omega_2 = 0 \tag{116}$$

$$s^2 + s(2\pi f_1 + 2\pi f_2) + (1 + A_0 \beta) 4\pi^2 f_1 f_2 = 0 \tag{117}$$

Note that eq. (117) has the form $as^2 + bs + c = 0$, and the roots can be found with the quadratic formula:

$$s = \frac{-b \pm \sqrt{b^2 - 4ac}}{2a} \tag{118}$$

i.e.,

$$s = -\frac{1}{2}(2\pi f_1 + 2\pi f_2) \pm \sqrt{(2\pi f_1 + 2\pi f_2)^2 - 16\pi^2 f_1 f_2 (1 + A_0 \beta)} \tag{119}$$

Eq. (119) gives two roots:

- The roots are a function of the feedback factor, β .
- Therefore, the roots will move as β increases from zero.
- We can plot a root locus!!!

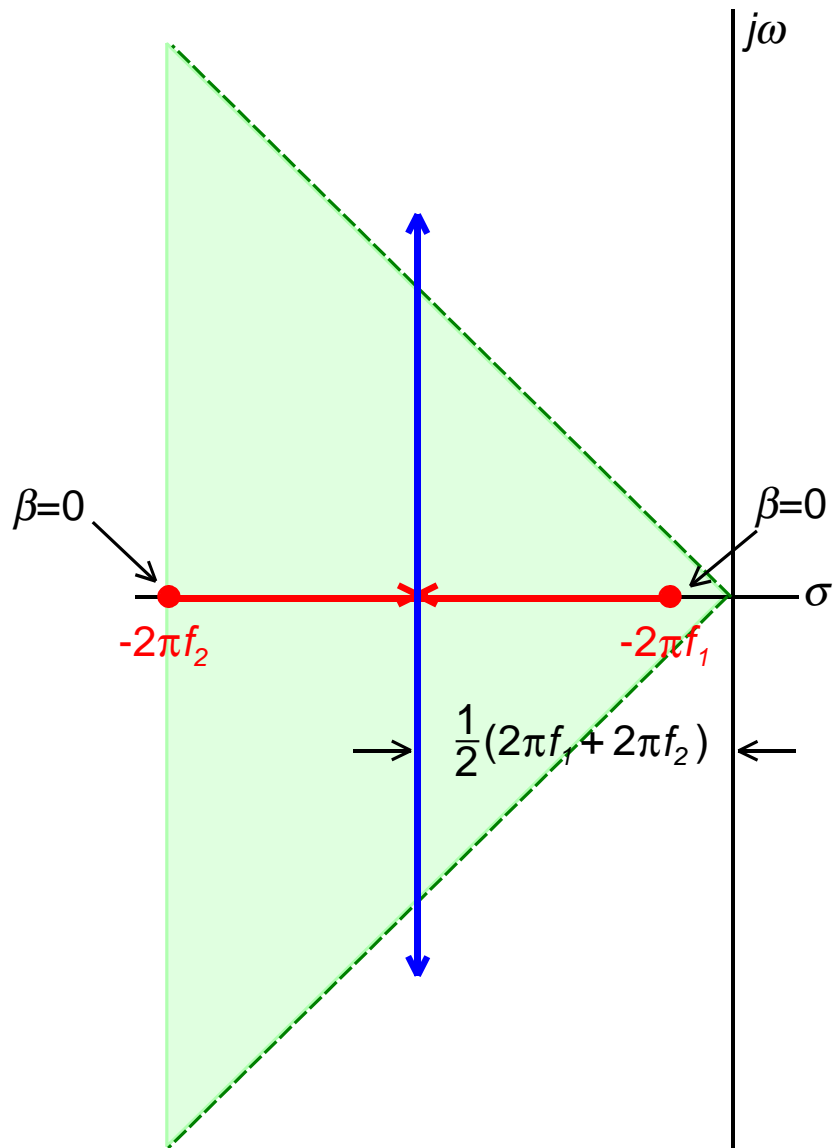


Fig. 92. Root locus of poles in a two-pole amplifier with negative feedback.

One can see that, as β increases from zero, the amplifier eventually exhibits excessive ringing (excessive gain peaking).

However, the poles never move into the right half-plane, i.e., the amplifier is always stable.

Amplifiers With 3 or More Poles

We'll illustrate the behavior of these amplifiers by example.

Consider an amplifier with an open-loop transfer function that has three identical poles on the negative real axis at $-2\pi f_b$:

$$A(s) = \frac{1000}{\left(\frac{s}{2\pi f_b} + 1\right)^3} \quad (120)$$

To find the closed-loop poles we need the roots of $1 + \beta A(s) = 0$, from which $\beta A(s) = -1$, i.e.:

$$\frac{1000\beta}{\left(\frac{s}{2\pi f_b} + 1\right)^3} = -1 \quad (121)$$

Taking the cube root of both sides of eq. (121):

$$\frac{10\sqrt[3]{\beta}}{\left(\frac{s}{2\pi f_b} + 1\right)} = \sqrt[3]{-1} \quad (122)$$

And solving for s to find the closed-loop poles:

$$s = 2\pi f_b \left(\frac{10\sqrt[3]{\beta}}{\sqrt[3]{-1}} - 1 \right) \quad (123)$$

But $(\sqrt[3]{-1} = -1)$, or $(\sqrt[3]{-1} = 1\angle 60^\circ)$, or $(\sqrt[3]{-1} = 1\angle -60^\circ)$.

So there are three closed-loop poles.

The three closed-loop poles are:

$$\begin{aligned} s_1 &= 2\pi f_b \left[10\sqrt[3]{\beta} (1\angle -60^\circ) - 1 \right] \\ s_2 &= 2\pi f_b \left[10\sqrt[3]{\beta} (1\angle 60^\circ) - 1 \right] \\ \text{and } s_3 &= -2\pi f_b \left[10\sqrt[3]{\beta} + 1 \right] \end{aligned} \quad (124)$$

The root-locus of these three poles as a function of the feedback factor, β , is shown below. Notice that, because poles move into the right half-plane, the amplifier eventually becomes unstable.

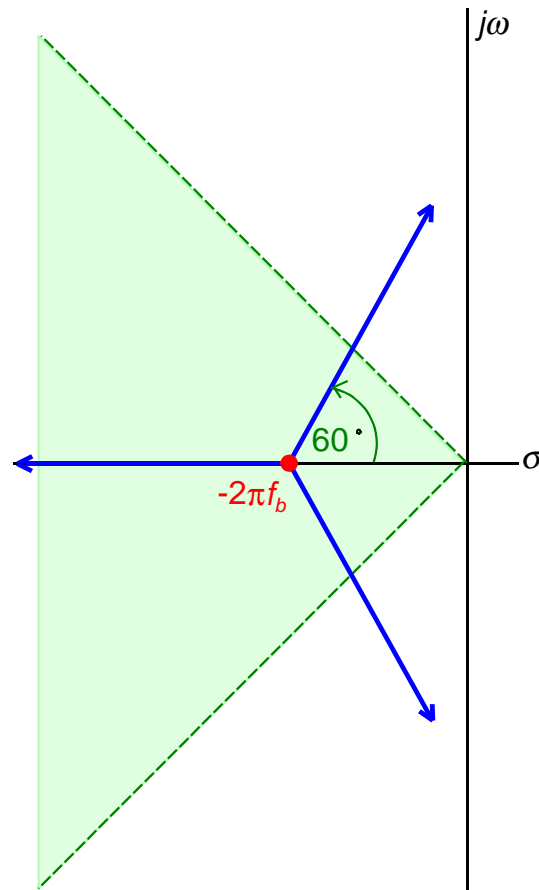


Fig. 93. Root locus of closed-loop poles in our 3-pole amplifier.

We will have a similar result for an amplifier with an open-loop transfer function that has four identical poles on the negative real axis at $-2\pi f_b$, because:

$$\begin{aligned} \sqrt[4]{-1} &= 1\angle 45^\circ & \sqrt[4]{-1} &= 1\angle -45^\circ \\ \sqrt[4]{-1} &= 1\angle 135^\circ & \sqrt[4]{-1} &= 1\angle -135^\circ \end{aligned} \quad (125)$$

Notice that with sufficient feedback, this amplifier becomes unstable also. We could extend this result to amplifiers with any larger number of poles.

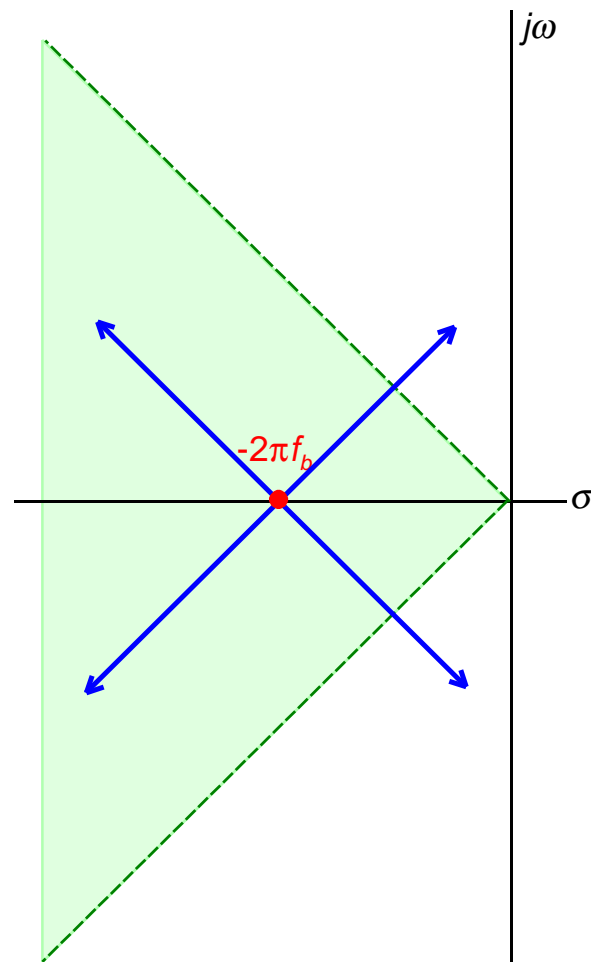


Fig. 94. Root locus of closed-loop poles in a 4-pole amplifier.

Gain Margin and Phase Margin

Introduction

Consider the closed-loop gain equation evaluated at $s = j2\pi f$:

$$A_f(s) = \frac{A(s)}{1 + \beta A(s)} \Rightarrow A_f(f) = \frac{A(f)}{1 + \beta A(f)} \quad (126)$$

where we have assumed β to be independent of frequency.

Now, suppose there is some particular frequency f_1 for which

$$\beta A(f_1) = -1 = 1 \angle \pm 180^\circ \quad (127)$$

For this case, we may conclude:

- The closed-loop gain $A_f(f_1)$ will be infinite.
- Poles will exist on the $j\omega$ axis.
- The transient response will have a constant-amplitude sinusoid!!!

In fact, what we have just described is an oscillator!!!

We will study oscillators in a subsequent section where this situation is desirable, but in an amplifier it is to be avoided!!!

Let's examine this situation more carefully:

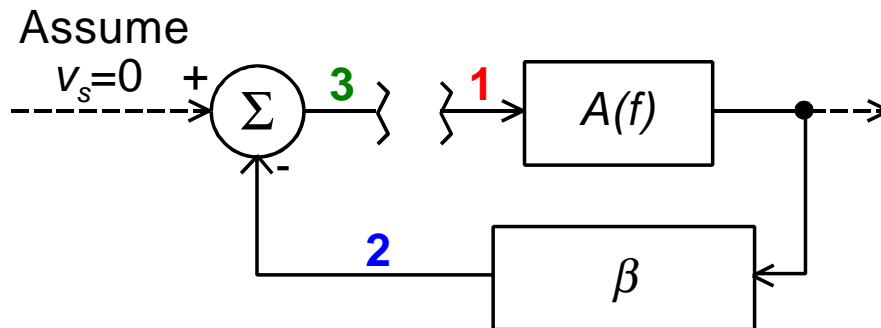


Fig. 95. Examining conditions for oscillation in a feedback amplifier.

1. Presume that a signal exists at the amplifier input (**1**):

$$V_m \cos 2\pi f_1 t \quad (128)$$

2. The output of the feedback network (**2**) is:

$$\beta A(f_1) \cdot V_m \cos 2\pi f_1 t = -V_m \cos 2\pi f_1 t \quad (129)$$

3. Then the signal applied to amplifier input (**3**) is:

$$0 - (-V_m \cos 2\pi f_1 t) = V_m \cos 2\pi f_1 t \quad (130)$$

4. Thus, the input signal can maintain itself, and we have a constant-amplitude sinusoid at the frequency f_1 !!!

Again, this is certainly a desirable condition in oscillators, but in an amplifier it is to be avoided!!!

Let's review the key point:

- Placing poles on the $j\omega$ axis requires $\beta A(f_1) = 1 \angle \pm 180^\circ$

More generally, we can observe what happens at the frequency for which $\angle \beta A(f_1) = \pm 180^\circ$:

- If the magnitude of $\beta A(f)$ is greater than 1, poles are in the right half-plane and the amplifier will be unstable.
- If the magnitude of $\beta A(f)$ is less than 1, poles are in the left half-plane and the amplifier will be stable.
- The lower the magnitude of $\beta A(f)$, the farther the poles are from the $j\omega$ axis, and the more stable the amplifier

Obviously, in an amplifier, we want to avoid placing poles on, or even near, the $j\omega$ axis!!!

Definitions

The value of the magnitude of $\beta A(f)$, when the phase angle of $\beta A(f) = \pm 180^\circ$ would be a good measure of amplifier stability:

Gain Margin: the amount that $20 \log |\beta A(f)|$ is below 0 dB, at the frequency where the angle of $\beta A(f) = -180^\circ$.

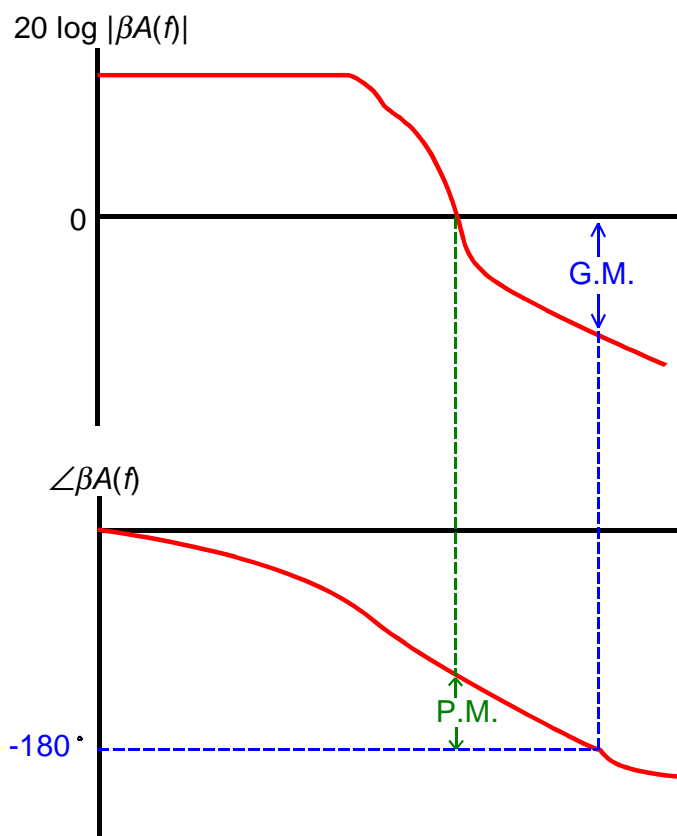
Another good measure of amplifier stability would be how close the angle of $\beta A(f)$ is to -180° when the magnitude of $\beta A(f) = 1$:

Phase Margin: the phase difference between the angle of $\beta A(f)$ and -180° , at the frequency where $20 \log |\beta A(f)| = 0$ dB.

Gain Margin, Phase Margin, and Bode Plots

Gain Margin and Phase Margin can be determined from the a Bode magnitude and phase plots. Note that:

$$20\log \beta A(f) = 20\log A(f) + 20\log \beta \quad (131)$$



Thus, magnitude plot of $\beta A(f)$ is just the magnitude plot of open-loop gain $A(f)$, shifted downward by $20 \log \beta$.

$\angle \beta A(f) = \angle A(f)$ because β is independent of frequency by assumption.

Thus, the phase plot of $\beta A(f)$ is same as the phase plot of $A(f)$.

Fig. 96. Illustration of gain margin and phase margin.

To avoid excessive ringing in the transient response, and excessive gain peaking in the frequency response, we generally require $G.M. \geq 10 \text{ dB}$ and $P.M. \geq 45^\circ$.

To repeat:

The magnitude plot of $\beta A(f)$ is just the magnitude plot of open-loop gain $A(f)$, shifted downward by $20 \log \beta$.

This would normally require us to take the $20 \log A(f)$ plot and redraw it on a new set of axes. This approach is tedious at best. But there is an easier way:

- Rather than shift the magnitude plot of $A(f)$ down by $20 \log \beta$, we can move the 0 dB axis up by $20 \log \beta$, i.e.,
- We can draw a “new axis” at $20 \log 1/\beta$.
- This is usually easy, because $1/\beta \approx A_f$.

We can show this mathematically. To determine phase margin, the point we want in Fig. 96 is where:

$$20 \log \beta A(f) = 20 \log \beta + 20 \log A(f) = 0 \quad (132)$$

or, where

$$20 \log A(f) = -20 \log \beta = 20 \log \frac{1}{\beta} \quad (133)$$

This is illustrated on the following page.

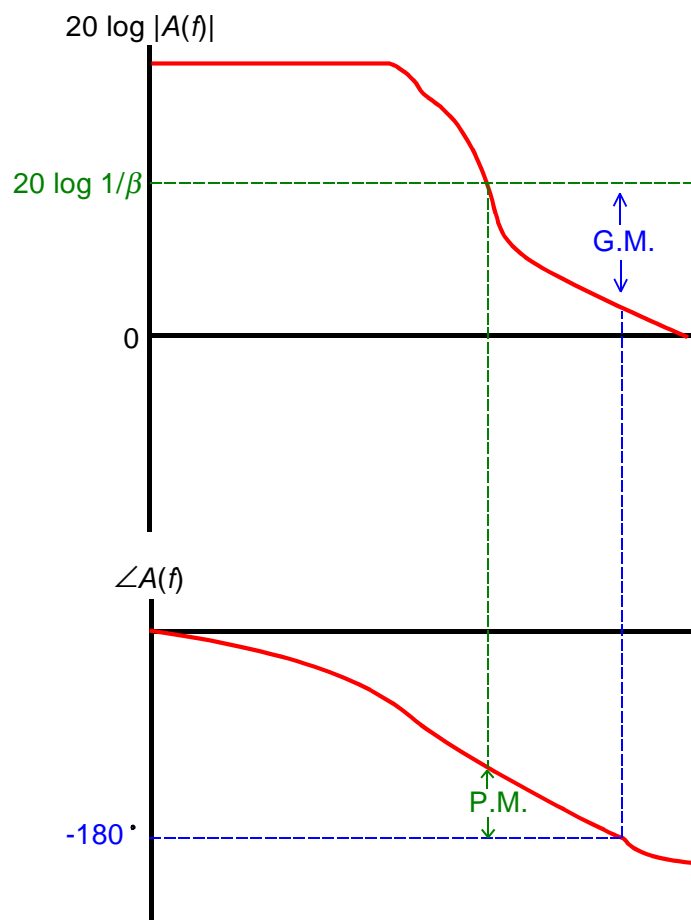


Fig. 97. Typical method of determining gain margin and phase margin.

Example #1

Given: An op amp with an open-loop dc gain of 1000, and three low-pass poles, all at 100 kHz.

Find: Maximum allowable feedback factor, β , for stability.

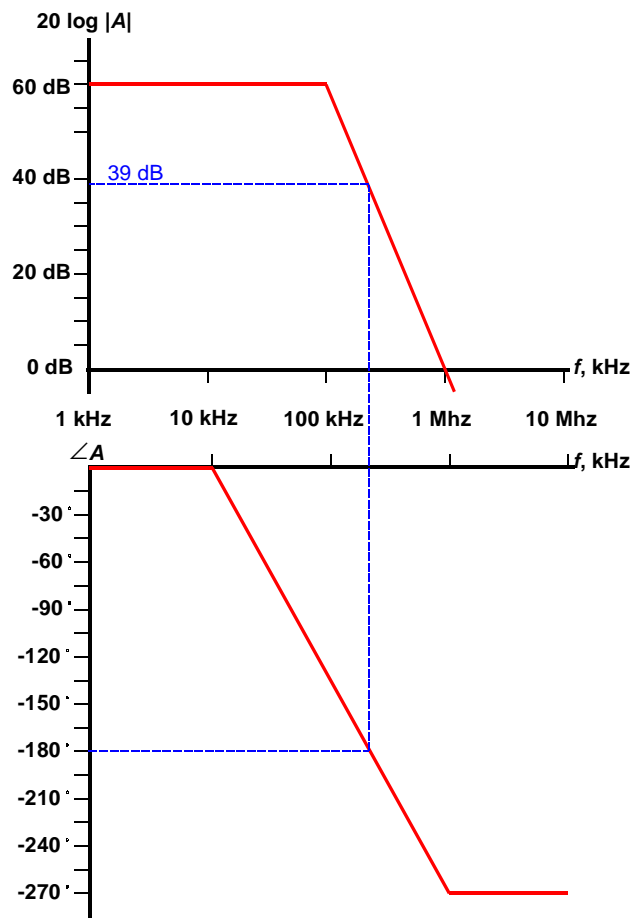


Fig. 98. G.M. and P.M. example #1.

- Solution:
1. Find frequency for which Phase Margin is 0° .
 2. Find open loop gain at this frequency (39 dB).
 3. Thus $20 \log 1/\beta = 39 \text{ dB}$ for P.M. = 0° .
 4. Solving gives $\beta \leq 0.0112$.

Example #2

Given: An op amp with an open-loop dc gain of 1000, and three low-pass poles, all at 100 kHz.

Find: Gain margin and phase margin for $\beta = 0.002$.

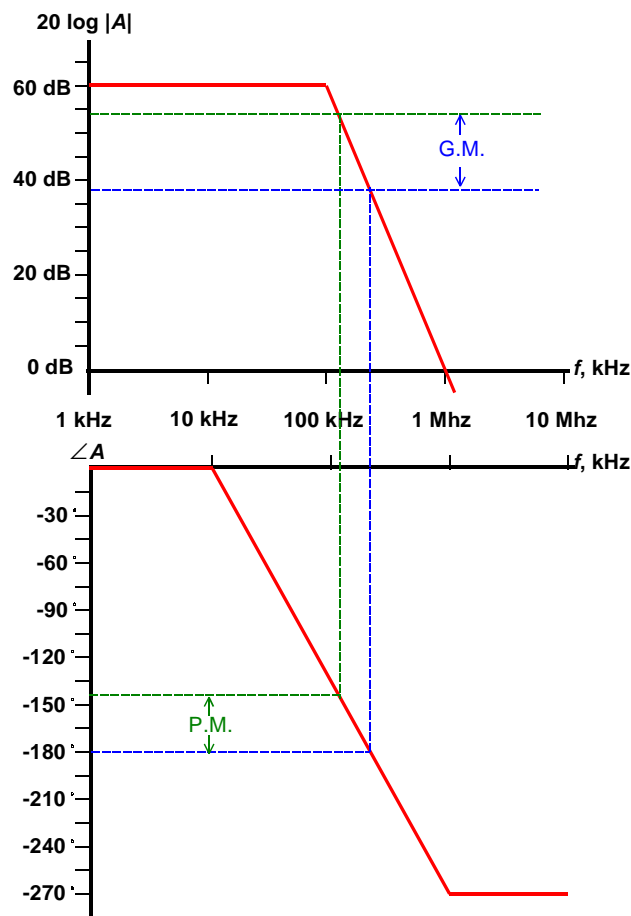


Fig. 99. G.M. and P.M. example #2.

- Solution:
1. Draw $20 \log 1/\beta$ line (at 54 dB) - note the frequency.
 2. Find phase shift at that frequency: P.M. = 36° .
 3. Find frequency for which phase shift is -180° .
 4. Find gain at that frequency: G.M. = 25 dB.

Example #3

Given: An op amp with an open-loop dc gain of 100 dB, and poles at 1 kHz, 100 kHz., and 10 MHz.

Find: Maximum β allowable for P.M. $\geq 45^\circ$.

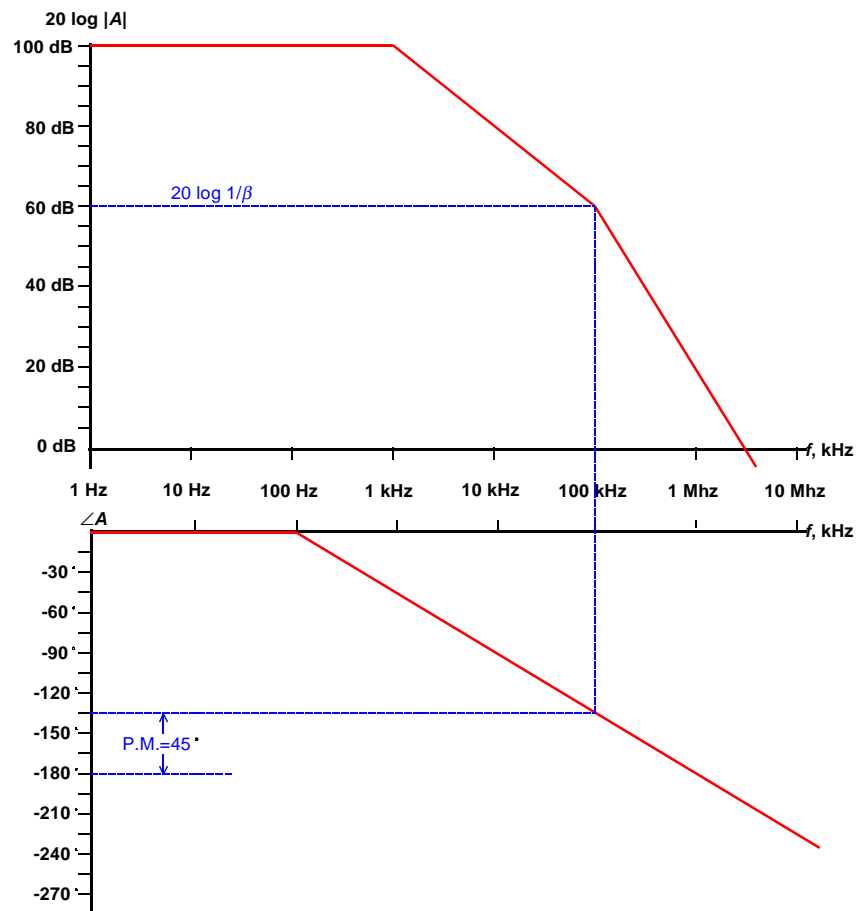


Fig. 100. G.M. and P.M. example #3.

- Solution:
1. Find frequency for which phase shift is -135° .
 2. Find gain at that frequency: $20 \log 1/\beta = 60$ dB.
 3. Solving gives $\beta = 0.001$.

Note in the previous example that the $20 \log 1/\beta$ line goes through 2nd pole on the magnitude plot. This is not just a coincidence!!!

If the poles are sufficiently spaced, the $20 \log 1/\beta$ line will *always* go thru the second pole for P.M. of 45° :

- This is because a P.M. of 45° corresponds to a phase shift of -135° .
- If we're "way past" the first pole we have -90° shift from that pole . . .
- . . . plus an additional -45° shift at the second pole, for a total phase shift of -135° .

This is why we determined that a P.M. of 45° produced acceptable stability in the first place !!!

Compensation of Amplifiers

Suppose we must use the open-loop amplifier from example #3 of the previous section . . .

$A_0 = 100$ dB; Poles at 1 kHz, 100 kHz., and 10 MHz

. . . in a closed-loop amplifier with a gain of 40 dB.

We also want the resulting feedback amplifier to be stable (P.M. $\geq 45^\circ$), but unfortunately, P.M. is only 21° :

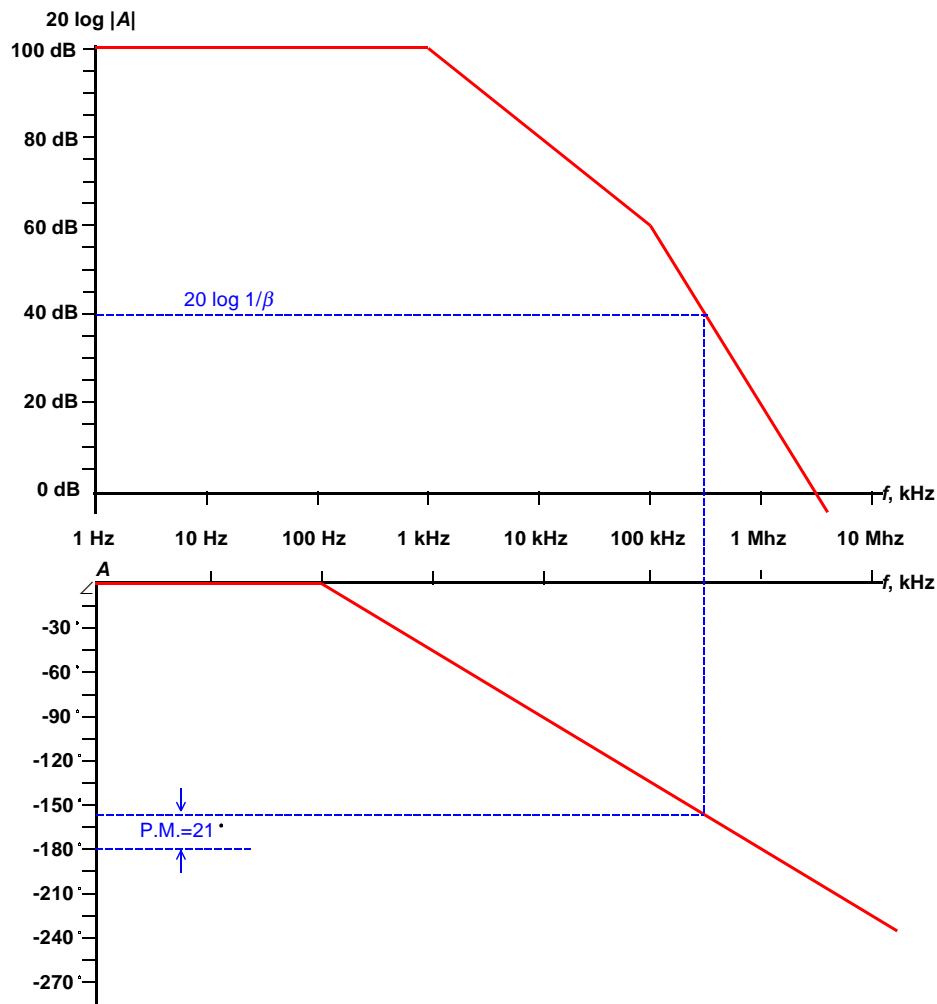


Fig. 101. Insufficiently stable amplifier.

Compensation by Adding a Dominant Pole

However, we can force P.M. to be 45° by adding another pole - a dominant pole.

To be dominant, the additional pole must be at a frequency much less than the current lowest pole (1 kHz), and the 1 kHz pole will become the second pole!!!

The $20 \log 1/\beta$ line will intersect the new magnitude plot at the second pole, like it always does for P.M. = 45° . Then we simply construct the new magnitude plot!!! In this case we need to add the dominant pole at 1 Hz:

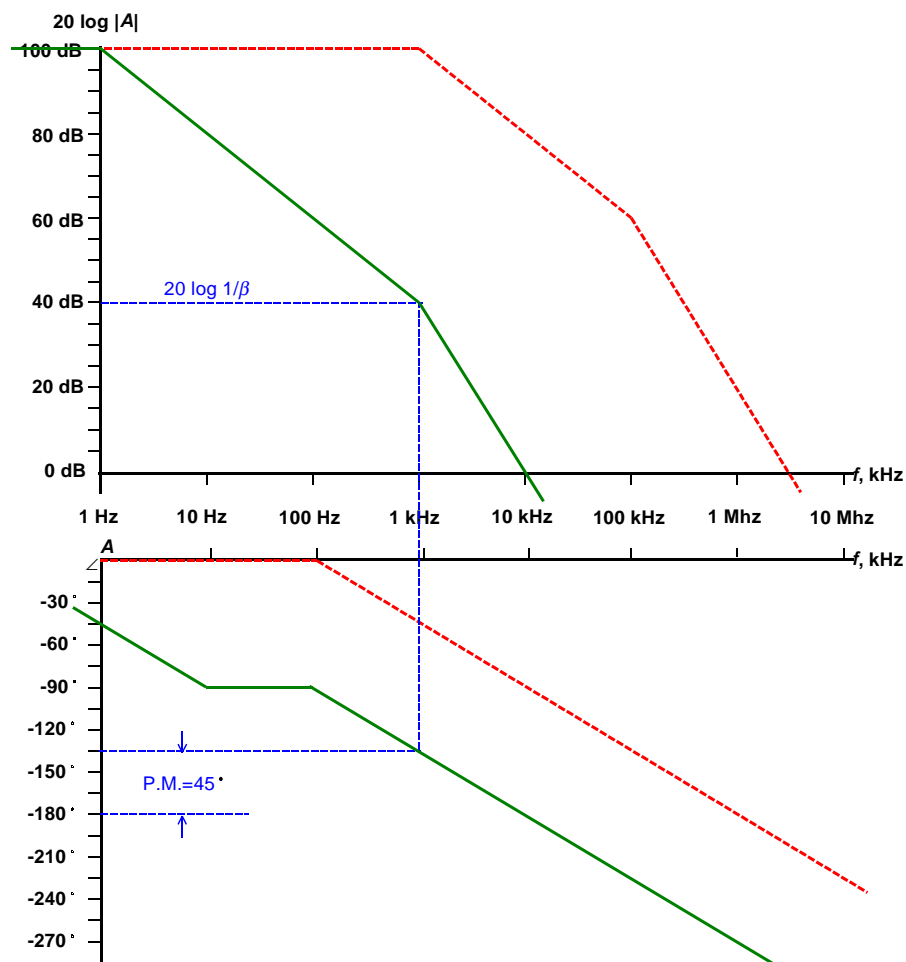


Fig. 102. Compensation by adding a dominant pole.

Adding a dominant pole is usually very simple:

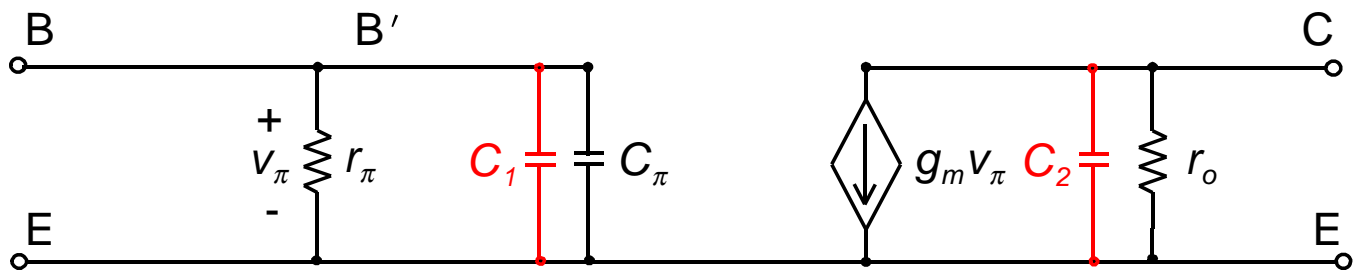


Fig. 103. A single capacitor, C_1 or C_2 , can be added to the open-loop amplifier to produce a dominant pole.

The drawback of this method is that we sacrifice a tremendous amount of bandwidth to achieve stability.

Compensation by Moving an Existing Pole

Instead of adding a dominant pole, we may be able to move an existing pole to a much lower frequency so that it becomes dominant.

The reduction in bandwidth with this approach is not as severe.

The least reduction in bandwidth results if the lowest existing pole is the one that can be moved - see the figure on the next page.

When we move the lowest pole, the second pole determines the frequency where the new P.M. = 45° , and we simply construct the new magnitude plot. The construction is shown on the following page.

To move a pole we need to identify (at least approximately) a capacitance that causes the pole we wish to move. We then move the pole by adding additional capacitance in parallel.

See the Bode diagram on the following page for details.

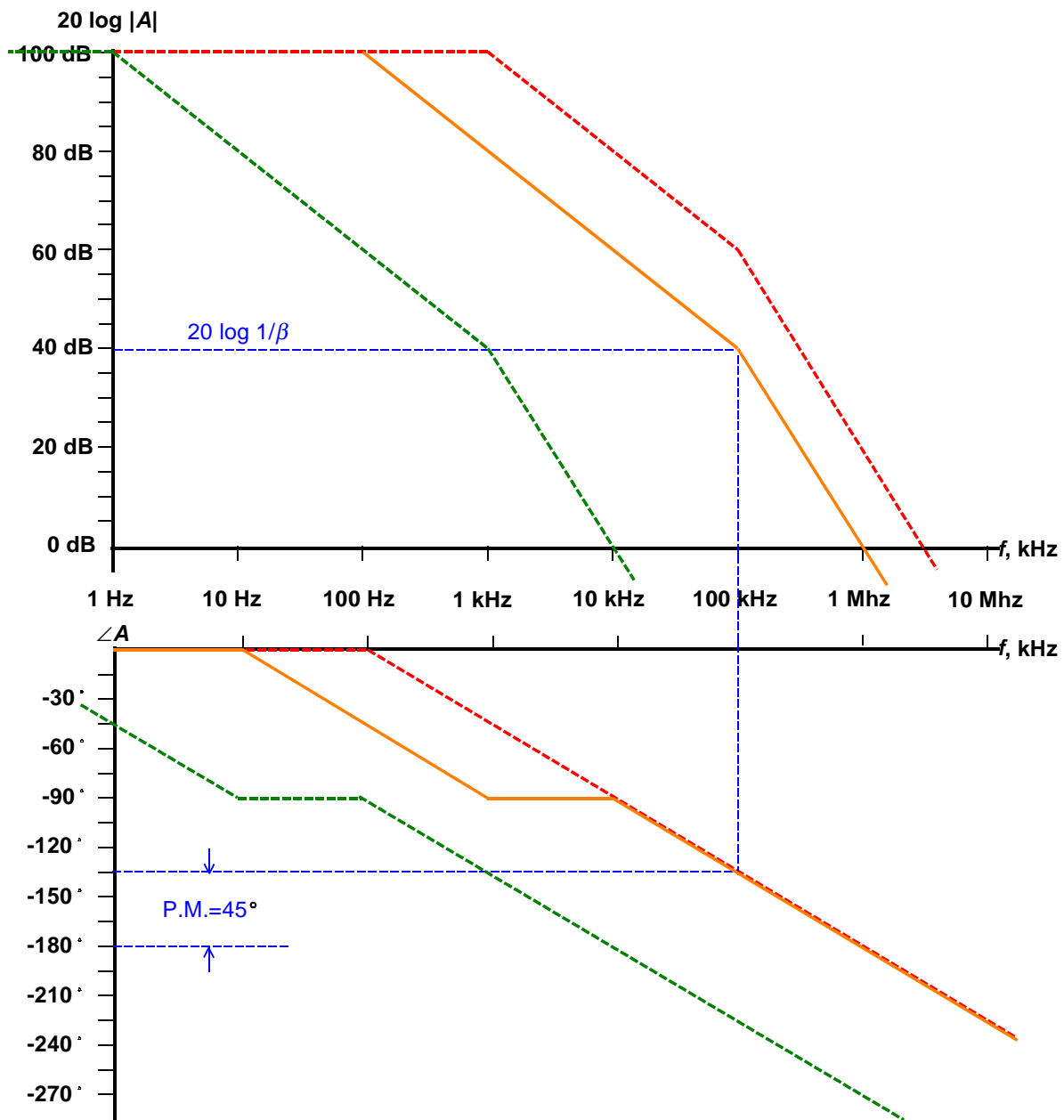


Fig. 104. Compensation by moving an existing pole. Note the less severe reduction in bandwidth compared to introducing an additional, dominant pole (here shown in dotted green for comparison).

Compensation by Adding a Pole and a Zero

Sometimes we can't move a pole directly, but we can cancel it with a zero, and add a new pole at the desired location.

The result is the same as moving that particular pole!!!

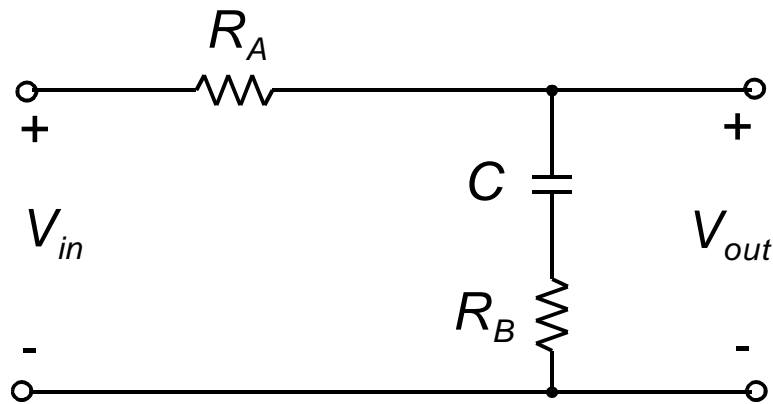


Fig. 105. Simple circuit with a pole and a zero in the transfer function.

The transfer function of the circuit in the figure above is:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{s}{2\pi f_z} + 1}{\frac{s}{2\pi f_p} + 1} \quad (134)$$

where

$$f_z = \frac{1}{2\pi R_B C} \quad \text{and} \quad f_p = \frac{1}{2\pi (R_A + R_B) C} \quad (135)$$

Compensation in the LM741 Operational Amplifier

The 30 pF capacitor in the LM741 introduces a dominant pole in the op amp (open loop) transfer function at approximately 5 Hz.

The dominant pole assures unconditional stability for feedback factors as large as 1, i.e., even for a voltage follower.

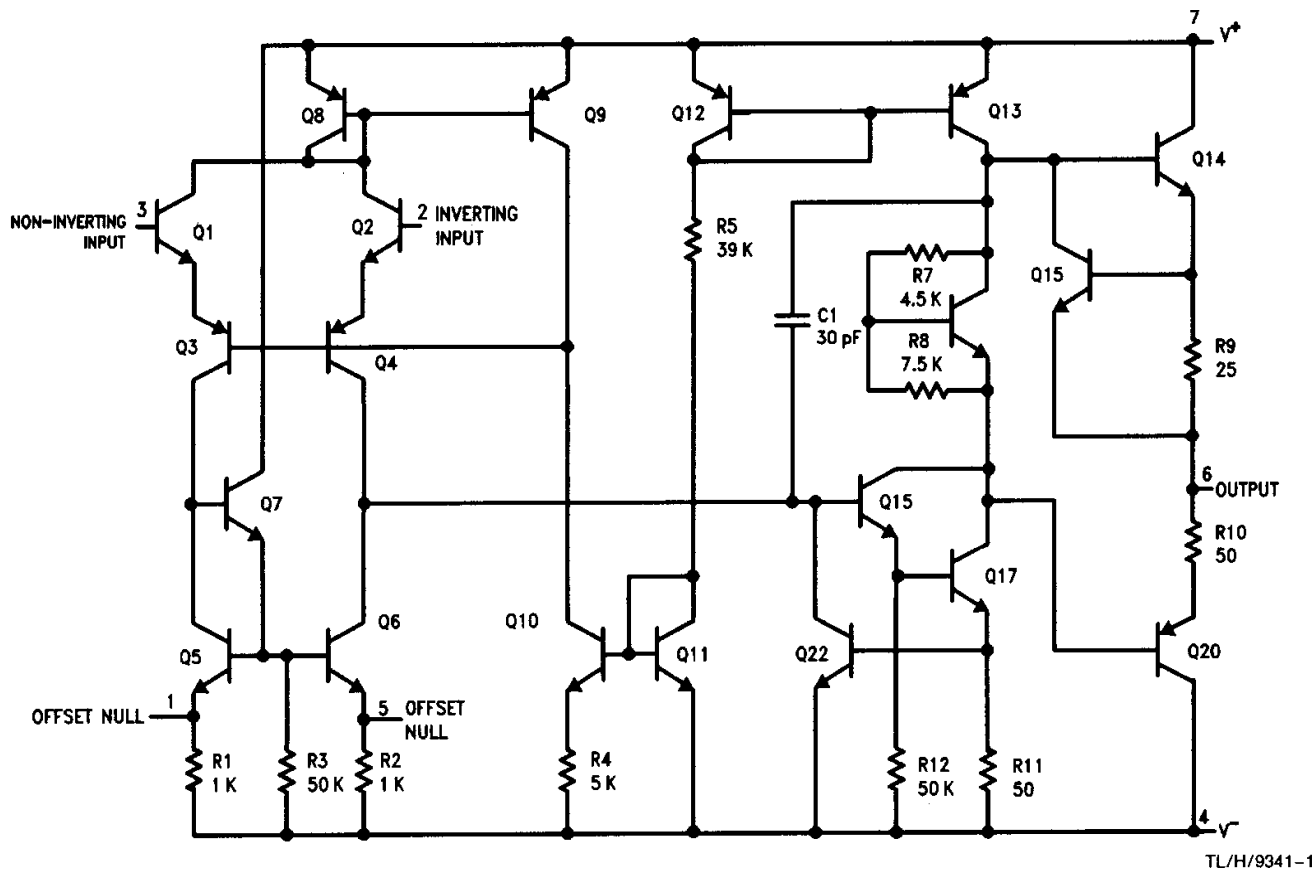


Fig. 106. Schematic diagram of the LM741 operational amplifier, obtained from National Semiconductor's web site at <http://www.national.com>.

The required capacitance is minimized by placing the capacitor at a point of large Thevenin resistance, and by using the Miller Effect to increase the effective capacitance.

Oscillators

Introduction

- Oscillators generate *periodic* signals - sine, square, etc.
- They convert dc power to ac power spontaneously.

- Examples are:

Local Oscillator - generates a sinusoidal signal used to select the proper frequency in a radio, TV, etc.

Clock - computer-generated rectangular waves for timing

- In switching oscillators, active devices are used as switches.
- In linear oscillators, active devices are used in a linear feedback amplifier.

The feedback path around the amplifier is usually intentionally frequency selective :

$$\beta = \beta(f) \quad (136)$$

We have just studied how to avoid oscillation in feedback amplifiers, but by doing so, we have also already studied how to produce oscillation.

Let's re-visit a part of our discussion of gain margin and phase margin from p. 67:

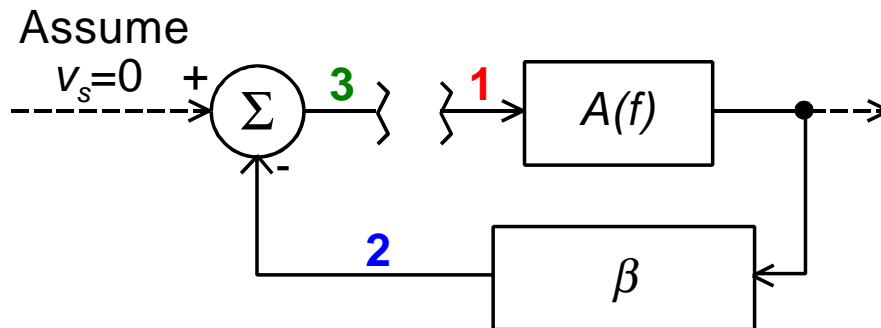


Fig. 107. Examining conditions for oscillation in a feedback amplifier (Fig. 95 repeated).

1. Presume that a signal exists at the amplifier input (**1**):

$$V_m \cos 2\pi f_1 t \quad (137)$$

2. The output of the feedback network (**2**) is:

$$\beta(f_1)A(f_1) \cdot V_m \cos 2\pi f_1 t = -V_m \cos 2\pi f_1 t \quad (138)$$

3. Then the signal applied to amplifier input (**3**) is:

$$0 - (-V_m \cos 2\pi f_1 t) = V_m \cos 2\pi f_1 t \quad (139)$$

4. Thus, the input signal can maintain itself, and we have a constant-amplitude sinusoid at the frequency f_1 !!!

We can build an oscillator if the gain “around the loop” is unity!!!

We usually don't need to identify the amplifier block, the feedback block, or the summing block. We need only concern ourselves with the gain around the loop.

(Don't confuse “gain around the loop” with “loop gain” which we already defined as the product $A(f)\beta(f)$)

The requirement of unity gain around the loop means:

- The magnitude of the gain around the loop equals 1.
- The total phase shift around the loop is 0° or $\pm 360^\circ$.

This is known as the Barkhausen Criterion.

Practical Linear Oscillators:

- Have a gain magnitude greater than unity so that oscillations will build.
 - Eventually, amplifier nonlinearity (“clipping”) changes the gain back to unity.
 - This assures oscillation will always begin despite component aging, temperature and humidity changes, etc.
-

RC Oscillator Example - Wien-Bridge Oscillator

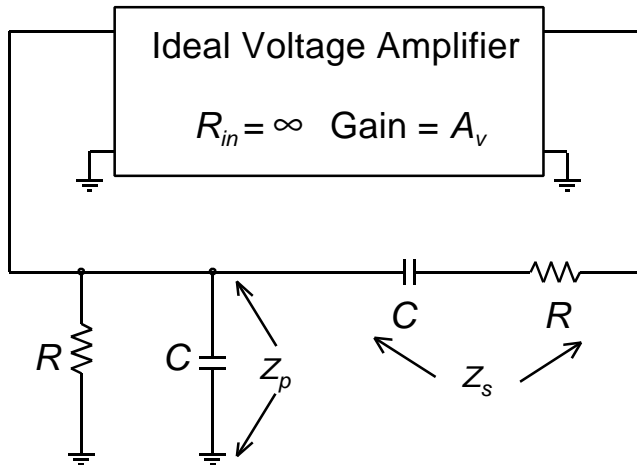


Fig. 108. Wien-Bridge Oscillator

Here, we will put the principles of the previous section to work. To analyze this circuit, we:

1. Break the loop at any convenient place.
2. Insert a test source.
3. Calculate gain all the way around the loop.

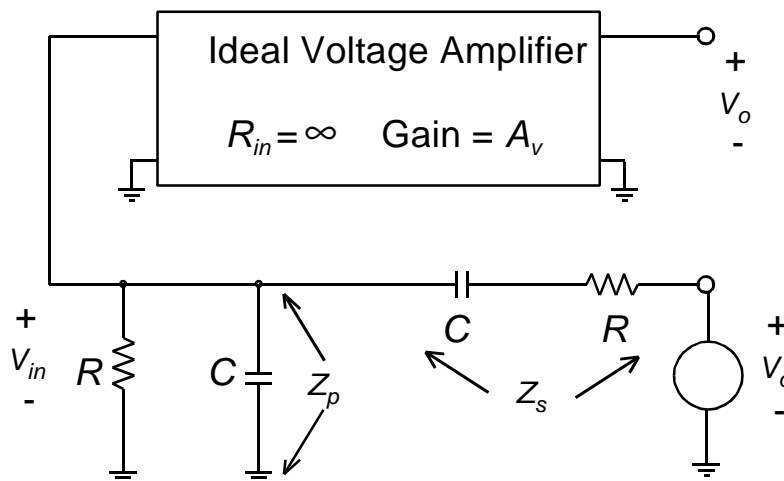


Fig. 109. Modified oscillator circuit, ready for gain calculation.

We'll start with the passive network & note that $R_{in} = \infty$, so:

$$\frac{V_{in}}{V_o} = \frac{Z_p}{Z_s + Z_p} = \frac{\frac{R(1/j\omega C)}{R + 1/j\omega C}}{R + 1/j\omega C + \frac{R(1/j\omega C)}{R + 1/j\omega C}} \quad (140)$$

Now, repeating eq. (?):

$$\frac{V_{in}}{V_o} = \frac{Z_p}{Z_s + Z_p} = \frac{\frac{R(1/j\omega C)}{R + 1/j\omega C}}{R + 1/j\omega C + \frac{R(1/j\omega C)}{R + 1/j\omega C}} \quad (141)$$

and multiplying the numerator and the denominator by $R + 1/j\omega C$:

$$\begin{aligned} \frac{V_{in}}{V_o} &= \frac{R\left(\frac{1}{j\omega C}\right)}{\left(R + \frac{1}{j\omega C}\right)^2 + R\left(\frac{1}{j\omega C}\right)} \\ &= \frac{R\left(\frac{1}{j\omega C}\right)}{R^2 + 2R\left(\frac{1}{j\omega C}\right) - \frac{1}{\omega^2 C^2} + R\left(\frac{1}{j\omega C}\right)} \\ &= \frac{R\left(\frac{1}{j\omega C}\right)}{\left(R^2 - \frac{1}{\omega^2 C^2}\right) + 3R\left(\frac{1}{j\omega C}\right)} = \frac{R}{j\omega CR^2 - j\frac{1}{\omega C} + 3R} \\ &= \frac{R}{3R + j\left(\omega CR^2 - \frac{1}{\omega C}\right)} \end{aligned} \quad (142)$$

Note that we have manipulated V_{in}/V_o so that all the frequency terms are in the denominator!!! This is a standard approach!!!

Let's catch our breath and review . . .

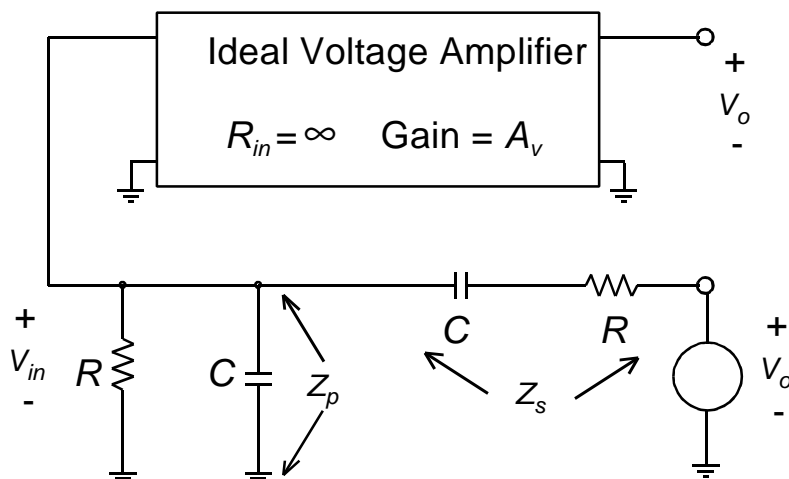


Fig. 110. Modified oscillator circuit, ready for gain calculation (Fig. 109 repeated).

We're working our way around the loop . . .

So far we've obtained the transfer function from our test source to the input of the ideal amplifier.

That transfer function is repeated here for convenience:

$$\frac{V_{in}}{V_o} = \frac{R}{3R + j\left(\omega CR^2 - \frac{1}{\omega C}\right)} \quad (143)$$

To complete the loop, we need only account for the amplifier gain, so our transfer function around the loop is:

$$\frac{V_o}{V_o} = \frac{A_v R}{3R + j\left(\omega CR^2 - \frac{1}{\omega C}\right)} = 1 \angle 0^\circ \quad (144)$$

where we have already applied the Barkhausen Criterion by choosing the voltage V_o for both sides of the "break" in the loop.

Be sure to take note of more than this particular equation. The method used here is quite standard in most oscillator problems!!!

To complete the analysis, we first repeat eq. (144):

$$\frac{V_o}{V_o} = \frac{A_v R}{3R + j\left(\omega CR^2 - \frac{1}{\omega C}\right)} = 1 \angle 0^\circ \quad (145)$$

Notice that transfer function must have zero phase shift, which means the imaginary term in the denominator must be zero. This allows us to determine the frequency of oscillation, which we'll denote as ω_{osc} :

$$\begin{aligned} \omega_{osc} CR^2 - \frac{1}{\omega_{osc} C} &= 0 \Rightarrow \omega_{osc}^2 C^2 R^2 - 1 = 0 \\ \Rightarrow \omega_{osc} &= \frac{1}{RC} \Rightarrow f_{osc} = \frac{1}{2\pi RC} \end{aligned} \quad (146)$$

And, at f_{osc} , the magnitude must be unity (or greater) to insure oscillation:

$$\frac{A_v R}{3R + j0} = 1 \Rightarrow A_v = 3 \quad (147)$$

Practical Wien-Bridge Oscillator #1:

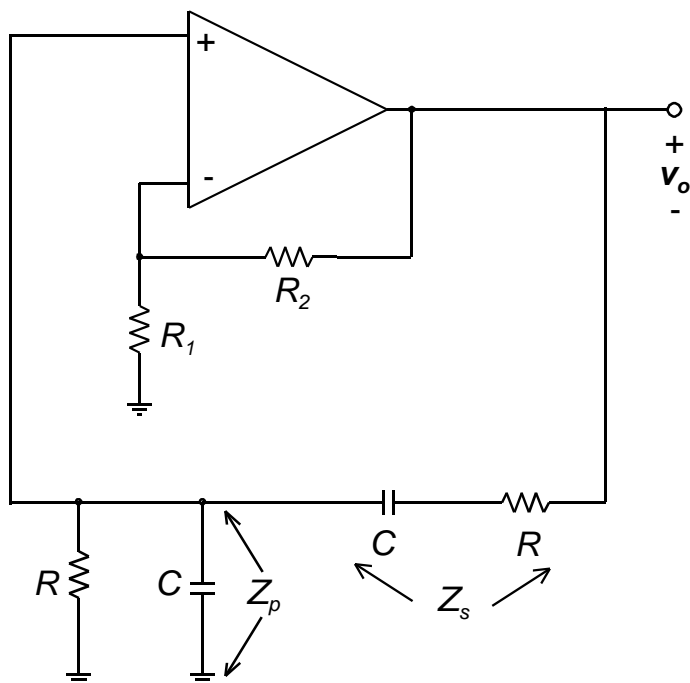


Fig. 111. Implementing the Wien-Bridge oscillator with an op amp.

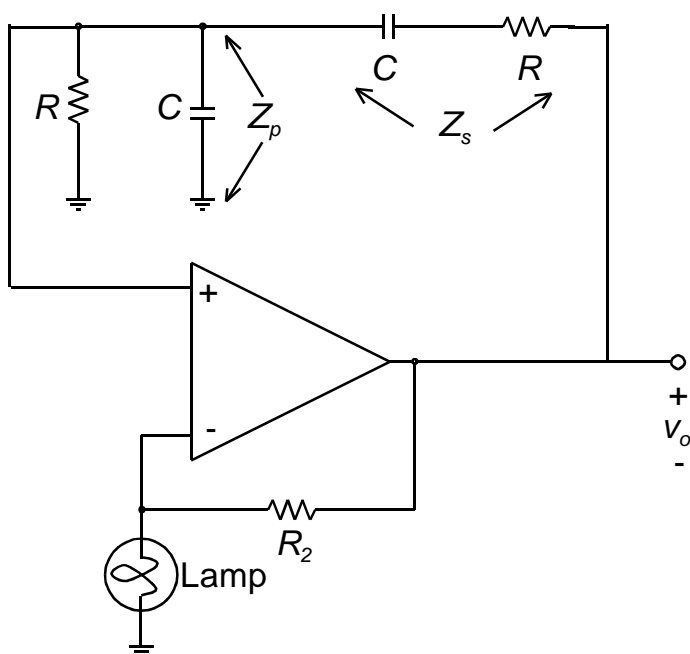


Fig. 112. A practical Wien-Bridge oscillator with AGC.

We can implement the Wien-Bridge oscillator by using an op amp with the gain set to be > 3 to insure oscillation will always begin (e.g. $R_2 = 22 \text{ k}\Omega$ and $R_1 = 10 \text{ k}\Omega$).

However, there is a problem: The oscillations grow until the op amp saturates.

This causes clipping of the output peaks at V_{OH} & V_{OL} .

The solution for this is to implement an automatic gain control (AGC).

In Fig. 112, the lamp filament has a low resistance when cold, and $A_v > 3$.

As oscillations begin to build, increasing current will flow through the lamp. The lamp resistance increases, and the gain is reduced automatically.

The drawback is that a very low value is required for R_2 , so the op amp is very heavily loaded.

Practical Wien-Bridge Oscillator #2:

We can implement the desired AGC in a different manner, as shown in Fig. 113.

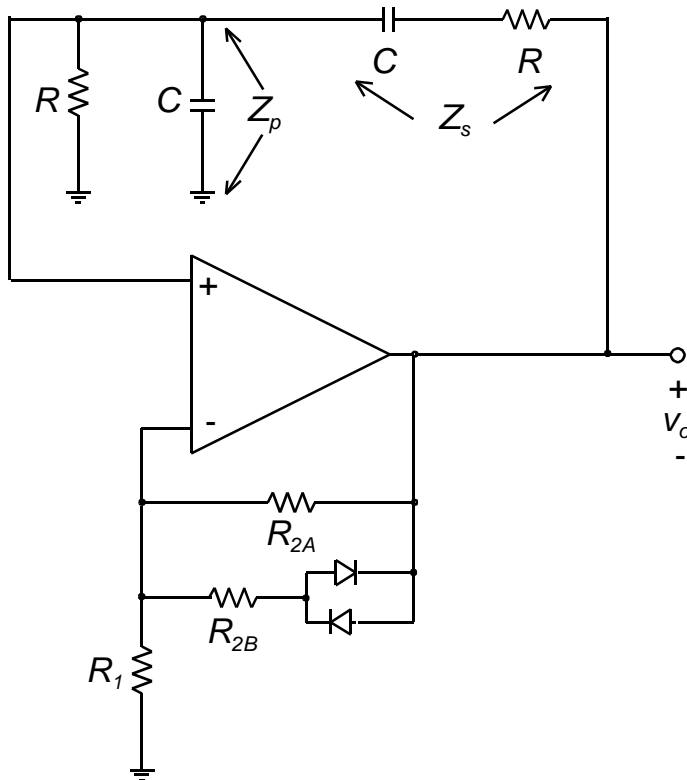


Fig. 113. A second Wien-Bridge oscillator with AGC.

In this circuit, at low output levels, $A_v = R_{2A}/R_1 > 3$. The diodes are off while the oscillation builds.

As oscillation grows, the diodes conduct, putting R_{2B} in parallel with R_{2A} .

Gain is reduced, and the output level stabilizes without clipping.

However, there's a drawback here, too. The nonlinear diodes introduce some distortion of their own.

Practical Wien-Bridge Oscillator #3:

The implementation of a fancier AGC circuit is our final Wien-Bridge oscillator.

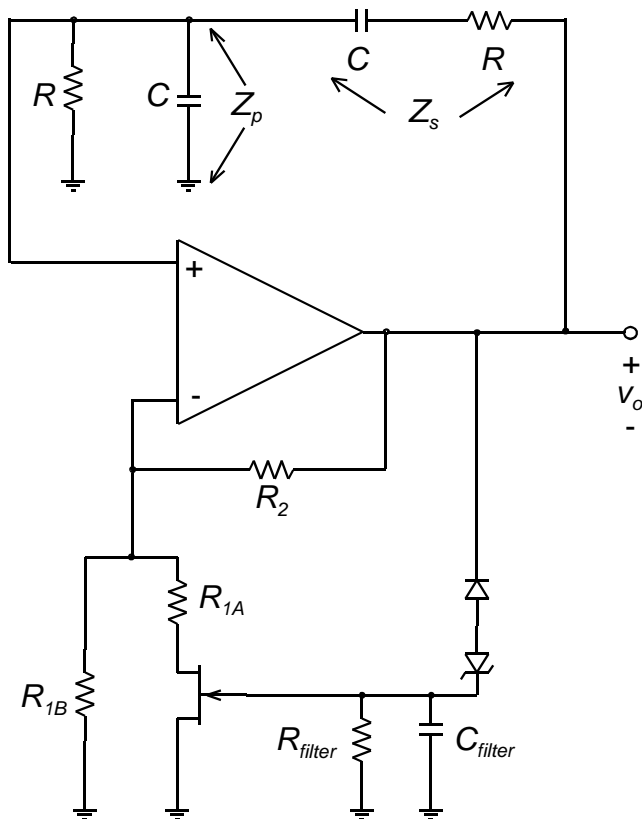


Fig. 114. Our last, and fanciest, Wien-Bridge oscillator with AGC.

The JFET is used in *its voltage controlled resistance* region:

R_{FET} is low for $V_{GS} \approx 0$.

R_{FET} is high for $V_{GS} < 0$.

The diodes, C_{filter} , and R_{filter} form a peak rectifier circuit:

The diodes conduct for $v_o < -(V_Z + 0.7 \text{ V})$.

C_{filter} stores negative voltage.

R_{filter} discharges C_{filter} slowly.

For low-amplitude oscillation, V_{GS} is near zero, and R_{FET} is small:

$$A_v = 1 + \frac{R_2}{R_{1B} \parallel (R_{1A} + R_{FET})} > 3 \quad (148)$$

For high-amplitude oscillation, V_{GS} is negative, and R_{FET} is large:

$$A_v \approx 1 + \frac{R_2}{R_{1B}} < 3 \quad (149)$$

LC Oscillators - The Hartley Oscillator

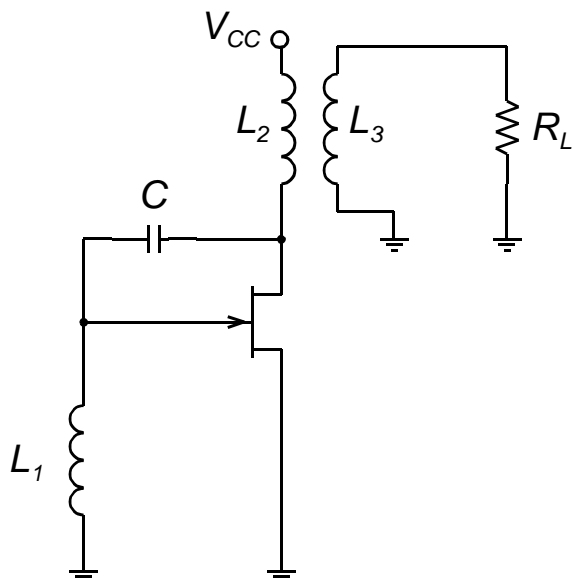


Fig. 115. Hartley oscillator.

Because inductances are less practical at low frequencies, LC oscillators are generally considered to be high-frequency (rf) oscillators.

For our analysis we note that:

R_L is reflected into the L_2 primary as R .

All elements are assumed to be ideal.

All device capacitances are ignored.

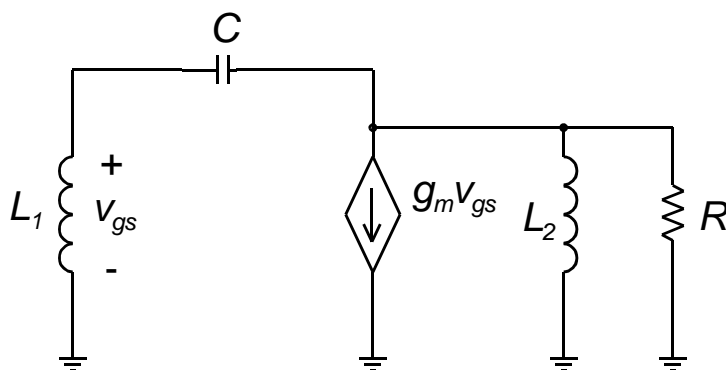


Fig. 116. Hartley oscillator small-signal equivalent.

We draw the small-signal model and recall that we want gain around the loop to be unity.

But its difficult to see a loop, so we redraw Fig. 116.

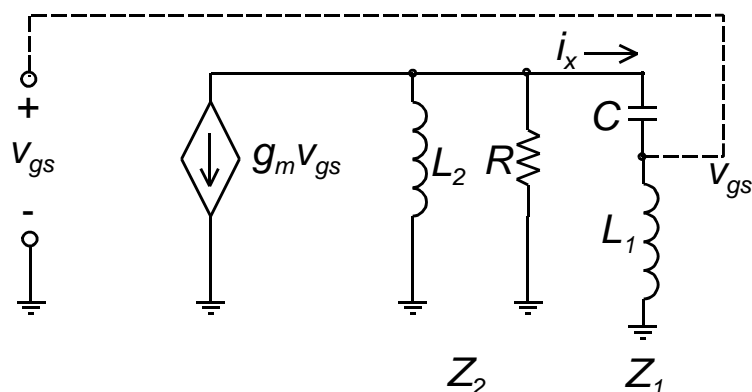


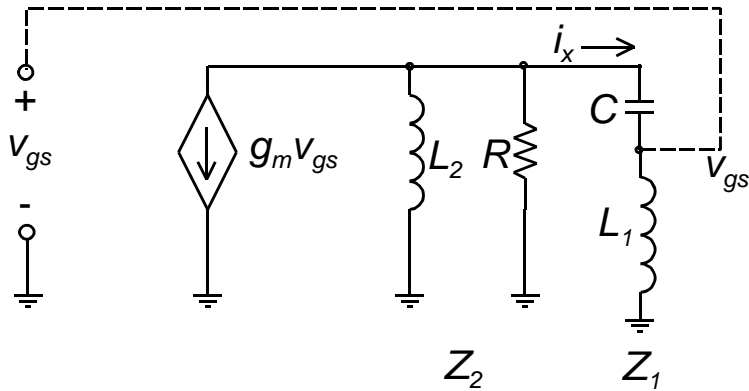
Fig. 117. Hartley equivalent redrawn.

For the analysis to proceed, note that:

Z_1 comprises L_1 and C in series.

Z_2 comprises L_2 and R in parallel.

Z_1 , Z_2 , and $g_m v_{gs}$ form a current divider.



The impedances are:

$$Z_1 = j \left(\omega L_1 - \frac{1}{\omega C} \right) \quad (150)$$

and

$$Z_2 = \frac{j\omega L_2 R}{R + j\omega L_2} \quad (151)$$

Fig. 118. Hartley equivalent redrawn (Fig. 117 repeated).

And the current divider equation is:

$$i_x = - \frac{Z_2}{Z_2 + Z_1} g_m v_{gs} \quad (152)$$

where

$$\begin{aligned} \frac{Z_2}{Z_2 + Z_1} &= \frac{\frac{j\omega L_2 R}{R + j\omega L_2}}{\frac{j\omega L_2 R}{R + j\omega L_2} + j \left(\omega L_1 - \frac{1}{\omega C} \right)} \\ &= \frac{j\omega L_2 R}{j\omega L_2 R + j\omega L_1 R - j \frac{R}{\omega C} + j^2 \omega^2 L_1 L_2 - j^2 \frac{L_2}{C}} \\ &= \frac{j\omega L_2 R}{\left(\frac{L_2}{C} - \omega^2 L_1 L_2 \right) + jR \left[\omega (L_1 + L_2) - \frac{1}{\omega C} \right]} \end{aligned} \quad (153)$$

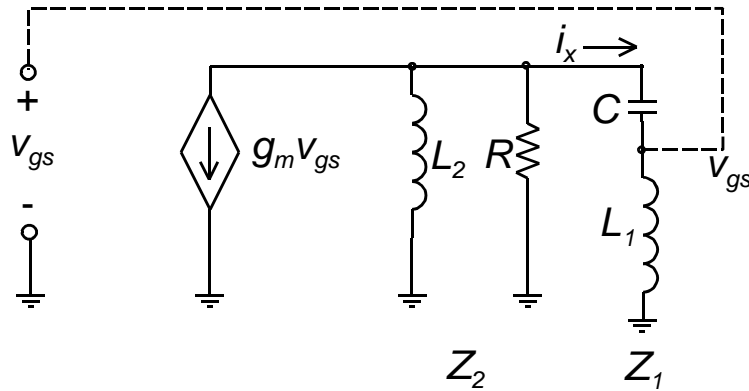


Fig. 119. Hartley equivalent redrawn (Fig. 117 repeated).

Now, repeating the current divider equation for convenience:

$$i_x = \frac{-j\omega L_2 R g_m v_{gs}}{\left(\frac{L_2}{C} - \omega^2 L_1 L_2\right) + jR\left[\omega(L_1 + L_2) - \frac{1}{\omega C}\right]} \quad (154)$$

Now, v_{gs} is the voltage across L_1 . It is simply $i_x(j\omega L_1)$:

$$v_{gs} = \frac{-(j\omega L_1) j\omega L_2 R g_m v_{gs}}{\left(\frac{L_2}{C} - \omega^2 L_1 L_2\right) + jR\left[\omega(L_1 + L_2) - \frac{1}{\omega C}\right]} \quad (155)$$

Multiplying the numerator terms together, and dividing both sides by v_{gs} , gives the familiar form:

$$1 \angle 0^\circ = \frac{\omega^2 L_1 L_2 R g_m}{\left(\frac{L_2}{C} - \omega^2 L_1 L_2\right) + jR\left[\omega(L_1 + L_2) - \frac{1}{\omega C}\right]} \quad (156)$$

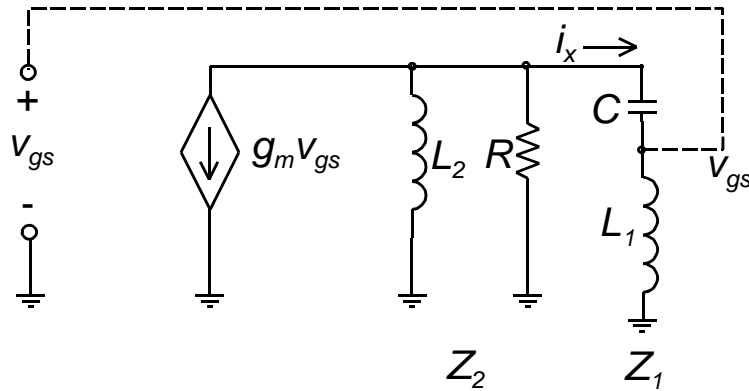


Fig. 120. Hartley equivalent redrawn (Fig. 117 repeated).

For 0° phase shift, the imaginary term in the denominator of eq. (156) must be zero:

$$\omega(L_1 + L_2) - \frac{1}{\omega C} = 0 \Rightarrow \omega(L_1 + L_2) = \frac{1}{\omega C} \quad (157)$$

$$\omega_{osc} = \frac{1}{\sqrt{(L_1 + L_2)C}}$$

And, for eq. (156) to have a magnitude of unity at ω_{osc} :

$$1 = \frac{\omega_{osc}^2 L_1 L_2 R g_m}{\frac{L_2}{C} - \omega_{osc}^2 L_1 L_2} \quad (158)$$

from which:

$$g_m = \frac{\frac{L_2}{C} - \omega_{osc}^2 L_1 L_2}{\omega_{osc}^2 L_1 L_2 R} = \frac{1}{\omega_{osc}^2 L_1 C R} - \frac{1}{R} \quad (159)$$

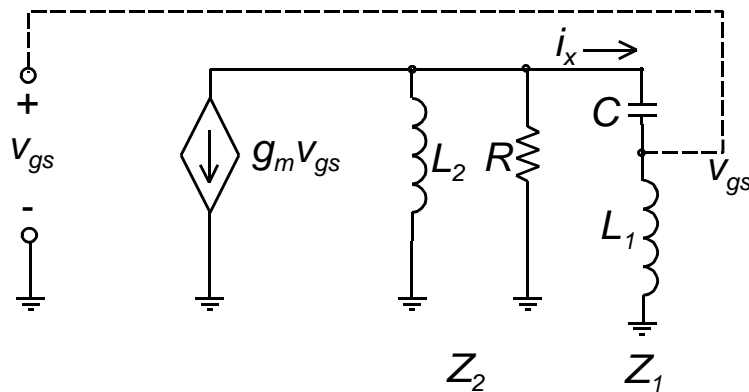
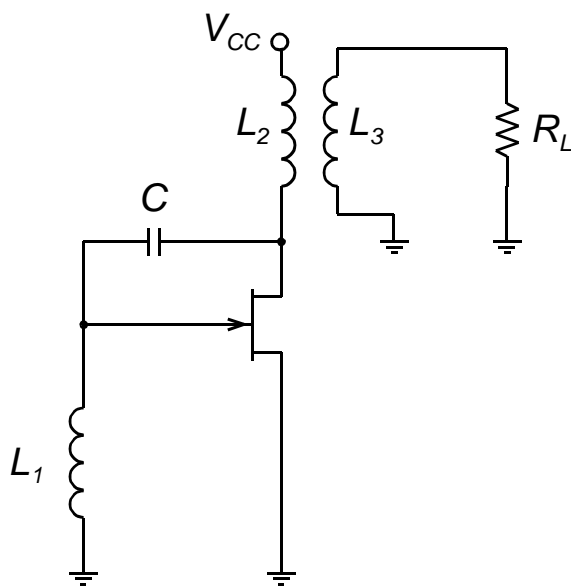


Fig. 121. Hartley equivalent redrawn (Fig. 117 repeated).

Finally, we substitute eq. (157) for ω_{osc}^2 in eq. (159):

$$g_m = \frac{1}{\frac{L_1 C R}{(L_1 + L_2) C}} - \frac{1}{R} = \frac{L_1 + L_2}{L_1 R} - \frac{L_1}{L_1 R} = \frac{L_2}{L_1 R} \quad (160)$$

We've done a lot of algebra!!! Let's review the original circuit, and the two important results:



$$\omega_{osc} = \frac{1}{\sqrt{(L_1 + L_2) C}} \quad (161)$$

$$g_m = \frac{L_2}{L_1 R} \quad (162)$$

Fig. 122. Hartley oscillator (Fig. 115 repeated).

LC Oscillators - The Colpitts Oscillator

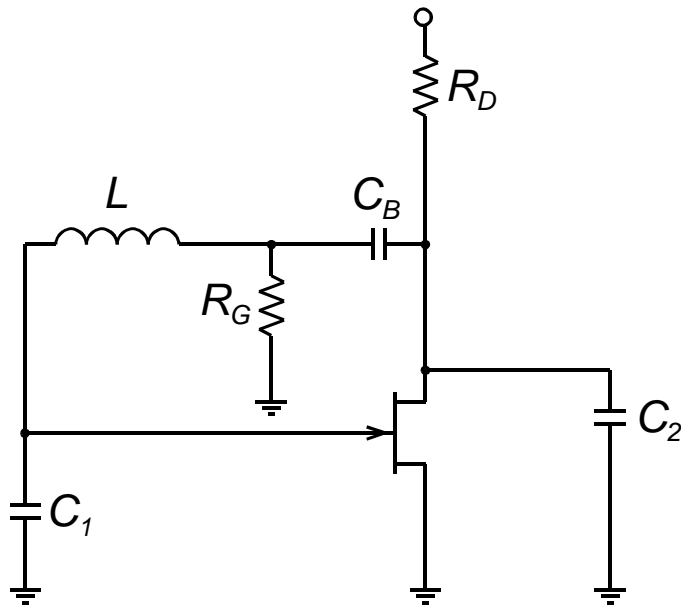


Fig. 123. Colpitts oscillator.

The Colpitts Oscillator is very similar topologically to the Hartley:

R_G provides a dc ground for gate.

C_B blocks dc drain voltage from the gate circuit, and provides an ac short circuit.

C_1 and C_2 can include device capacitances.

The small-signal equivalent circuit is shown below:

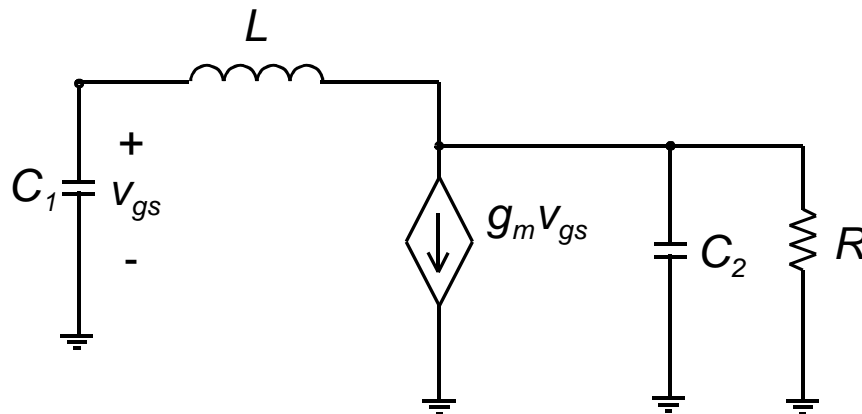


Fig. 124. Colpitts oscillator small-signal equivalent.

Again, note the similarity to Hartley oscillator. The analysis proceeds in a similar fashion. We show only the results here:

$$\omega_{osc} = \sqrt{\frac{C_1 + C_2}{LC_1C_2}} \quad \text{and} \quad g_m = \frac{C_1}{C_2R} \quad (163)$$

Hartley - Colpitts Comparison

Hartley Oscillator

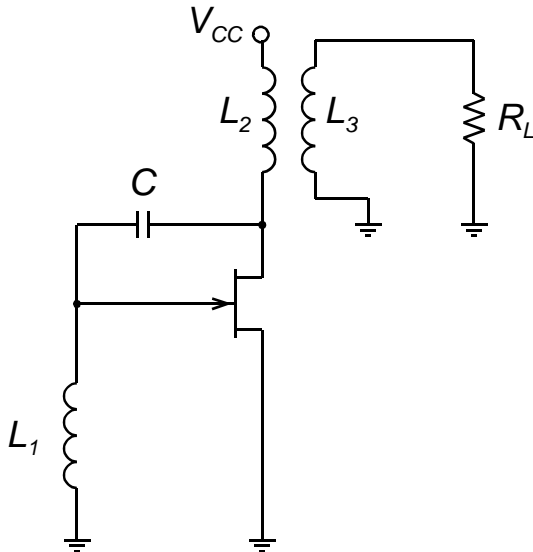


Fig. 125. Hartley oscillator (Fig. 115 repeated).

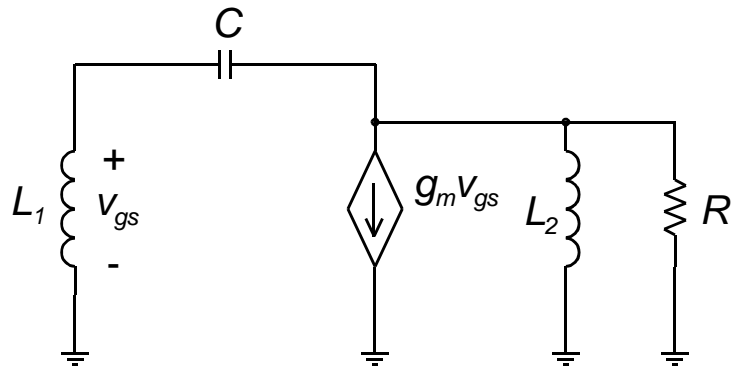


Fig. 126. Hartley oscillator small-signal equivalent (Fig. 116 repeated).

$$\omega_{osc} = \frac{1}{\sqrt{(L_1 + L_2)C}} \quad g_m = \frac{L_2}{L_1 R} \quad (164)$$

Colpitts Oscillator

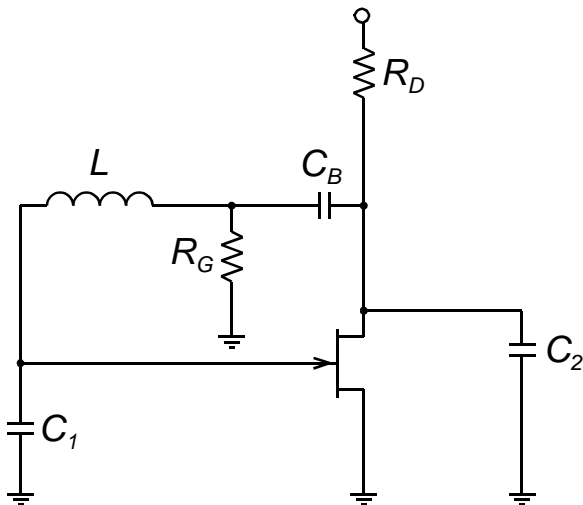


Fig. 127. Colpitts oscillator (Fig. 123 repeated).

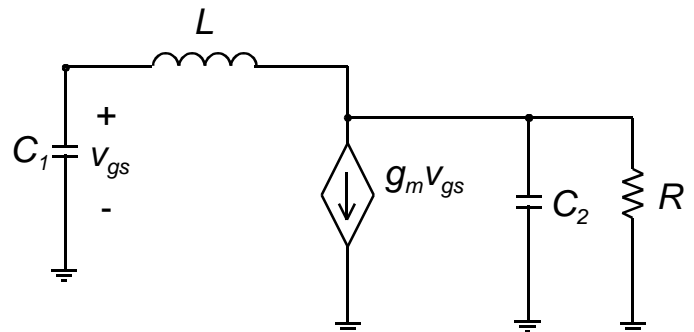


Fig. 128. Colpitts oscillator small-signal equivalent (Fig. 124 repeated).

$$\omega_{osc} = \sqrt{\frac{C_1 + C_2}{LC_1 C_2}} \quad g_m = \frac{C_1}{C_2 R} \quad (165)$$

Crystal Oscillators

The Piezoelectric Effect:

The piezoelectric effect describes the phenomenon whereby a mechanical stress applied to certain crystals produces a voltage proportional to the applied stress - the phenomenon is reciprocal.

The phenomenon was proven to exist in the early 1880's by the Curie brothers, who performed experiments with tourmaline, Rochelle salt, and cane sugar in addition to the now-well-known quartz crystals.

Piezoelectric crystals are used in various transducers, e.g., microphones, strain gauges, and phonograph cartridges (does anyone remember these???)

We'll look only at the use of piezoelectric crystals in oscillators.

Quartz Crystal Characteristics:

The electro-mechanical resonance characteristics of quartz crystals are *extremely* stable.

RC and LC oscillators are stable to within 100 - 1000 ppm

Crystal oscillators are stable to within 1 ppm !!!

Depending on the mode of mechanical vibration employed, crystal oscillators can be obtained with resonant frequencies from a few kHz to several hundred MHz.

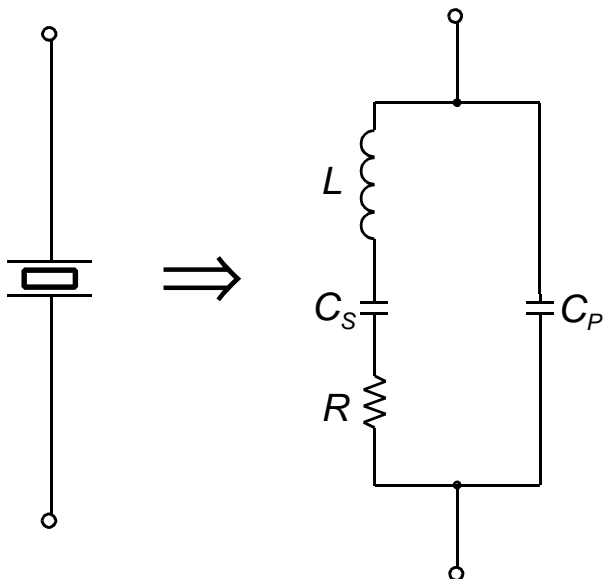


Fig. 129. Quartz crystal schematic symbol and equivalent ckt.

In the quartz crystal equivalent circuit at left, L , C_S , and R represent the electro-mechanical properties of the crystal.

$L \Rightarrow$ as high as to 100's of H

$C_S \Rightarrow$ as low as a fraction of a μF

$R \Rightarrow$ usually only a few 10's of Ω

$C_P \Rightarrow$ capacitance between electrodes, usually 1 - 10 pF

The quality factor, Q , is defined for a series circuit as $\omega L/R$. Conventional LC circuits at resonance have a Q of 200 to 300, but for a crystal at resonance, Q can be several 100,000 !!!

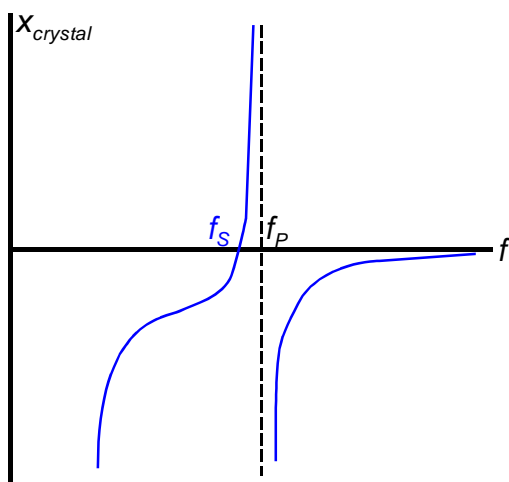


Fig. 130. Reactance of a quartz crystal.

The reactance of a quartz crystal is shown at left.

The series-resonant frequency, f_S , is where L and C_S resonate.

Above f_S , the series branch becomes inductive.

The parallel-resonant frequency, f_P , is where this inductance resonates with C_P .

Because of the high Q , f_S and f_P are within a few tenths of a %.

Pierce Oscillator

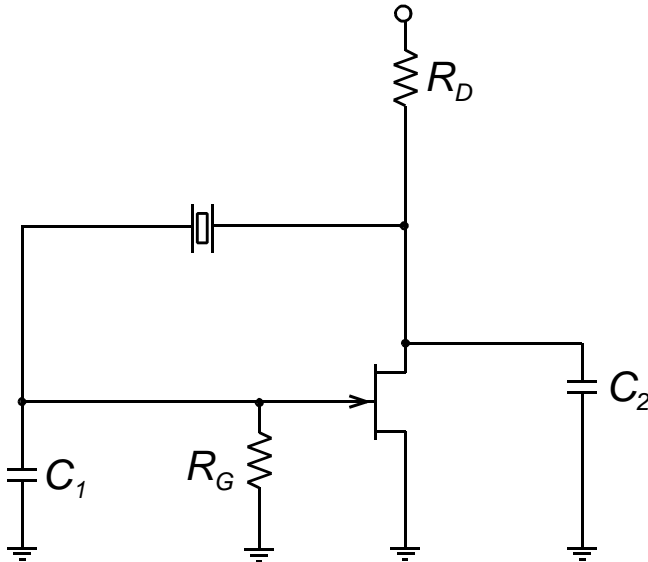


Fig. 131. Pierce oscillator.

The Pierce Oscillator is an example of an antiresonant oscillator - the crystal is used as inductance.

The circuit is simply a Colpitts oscillator with L replaced by the crystal.

Zero dc gate bias is provided by the resistance R_G .

The frequency of oscillation is between f_s and f_p .

Series-Resonant Crystal Oscillator

This is based on the Common-Base Colpitts Oscillator. The base is grounded, resulting in sufficient gain for oscillation, only at the crystal resonant frequency.

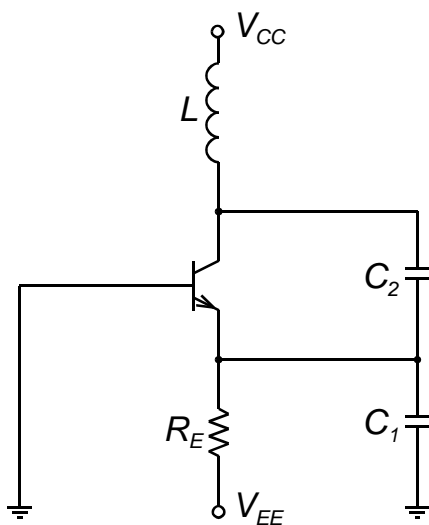


Fig. 132. Common-base Colpitts oscillator.

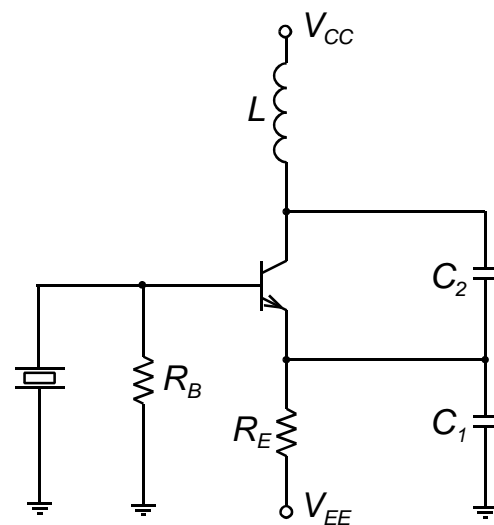


Fig. 133. Series-resonant crystal oscillator.

Comparators and Schmitt Triggers

Comparators

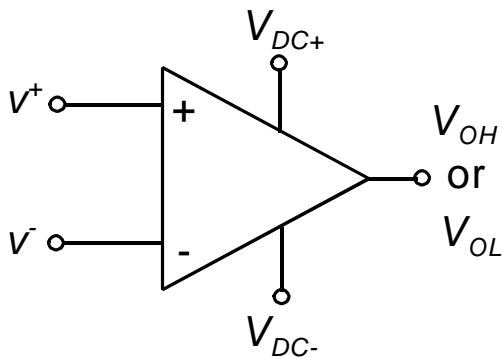


Fig. 134. Comparator.

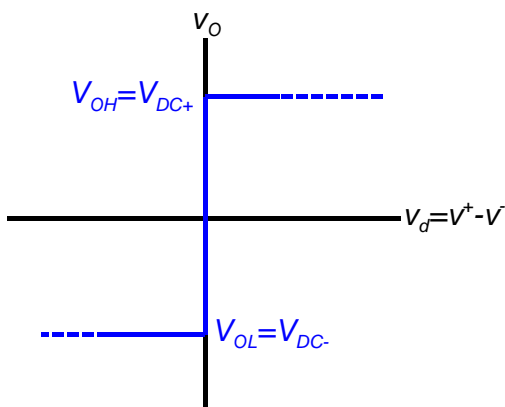


Fig. 135. Ideal transfer characteristic.

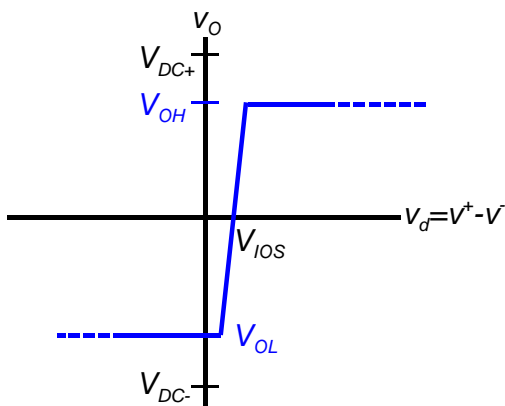


Fig. 136. Actual transfer characteristic.

A comparator is a linear amplifier, like an op amp, but intended for switching rather than for use in the linear region with negative feedback.

The output switches from V_{OH} to V_{OL} , i.e., from one saturated state to the other.

Ideal Transfer Characteristic:

Infinite gain

V_{IOS} , input offset voltage, = 0

$|v_d|$ for switching = 0

Infinite input impedance

Infinite speed:

$$t_d = t_r = t_s = t_f = 0$$

Actual Transfer Characteristic:

Finite gain (60 dB typical)

V_{IOS} usually a few mV

$|v_d|$ for switching < 1 mV

Finite speed

Speed vs. Overdrive:

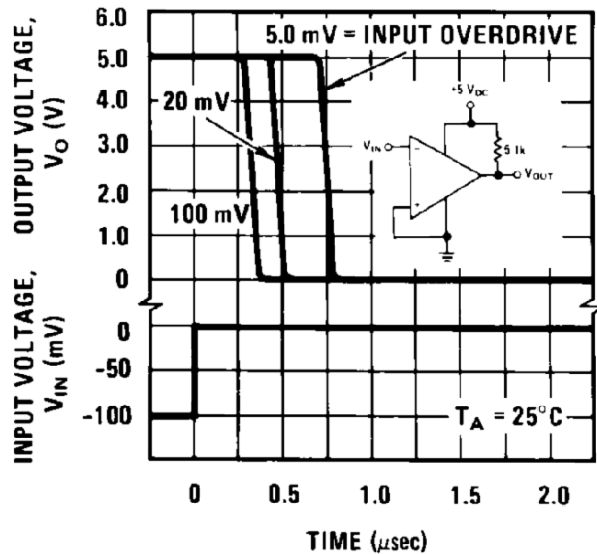


Fig. 137. Speed vs. overdrive, negative output transition, National LM393 comparator.

Overdrive is defined as the amount by which a step change in the input goes past zero.

The larger the overdrive, the faster the output transition.

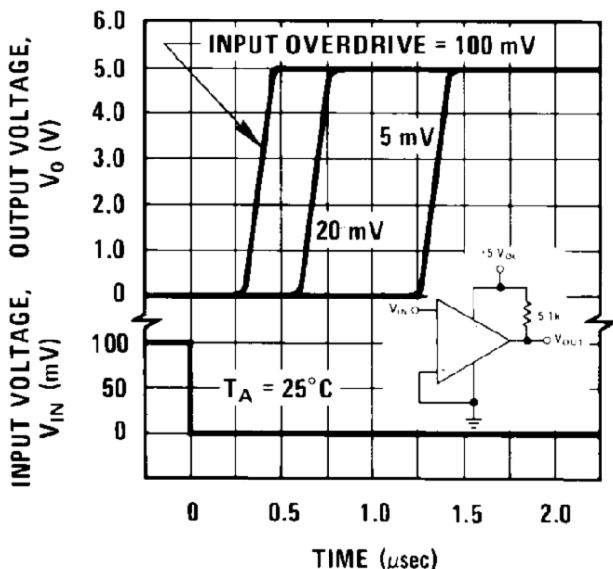


Fig. 138. Speed vs. overdrive, positive output transition, National LM393 comparator.

The effect of overdrive on the speed of the output transition is different for a negative-going output than for a positive-going output.

Figs. 137 and 138 are taken from the LM393 data sheets, available from National Semiconductor, Inc., at <http://www.national.com>.

Open-Loop Comparators:

The two possible configurations and their idealized output characteristics are shown.

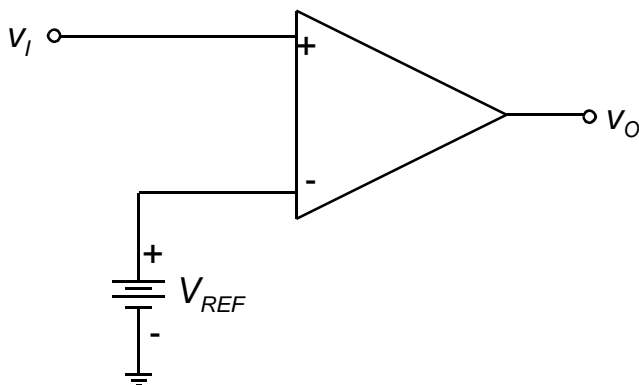


Fig. 139. Noninverting open-loop comparator

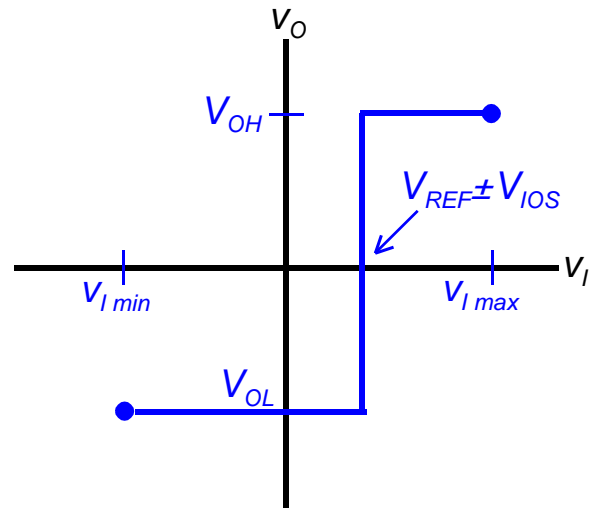


Fig. 140. Noninverting transfer function.

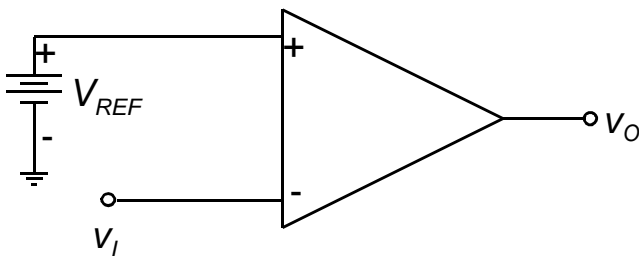


Fig. 141. Inverting open-loop comparator.

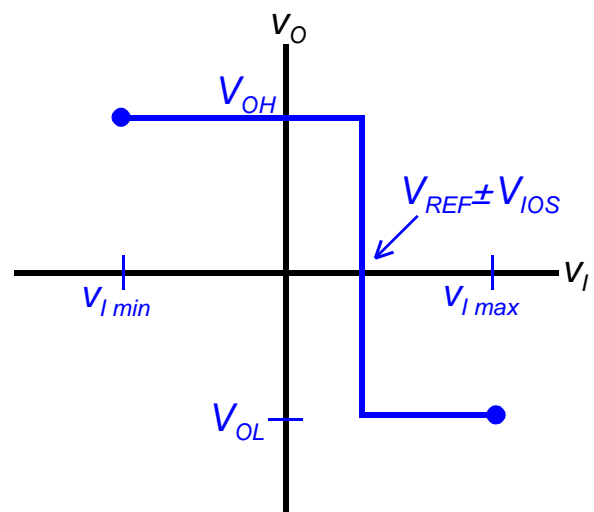


Fig. 142.
Inverting transfer function.

Comparators are not compensated. When operated “open-loop” a slowly varying input will likely result in an oscillating output, because the device is in the linear region long enough for oscillations to build.

Totem-Pole vs. Open Collector Outputs:

IC comparators have one of two output stages.

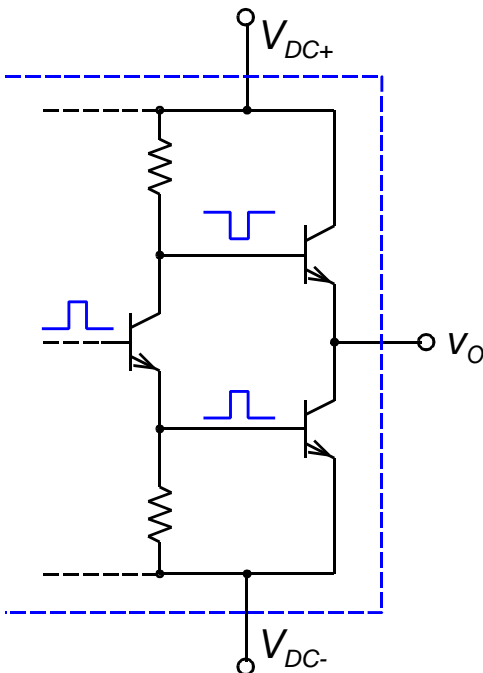


Fig. 143. Totem-pole output.

A totem-pole output, also called an “active pull-up,” is shown at left.

Advantages are:

Fast switching

$$V_{OH} \approx 0.7 \text{ V to } 1 \text{ V below } V_{CC}$$

$$V_{OL} \approx V_{CE \text{ sat}}$$

The major disadvantage is that it consumes power. Because transistors turn off more slowly than they turn on, a large current spike occurs at each transition.

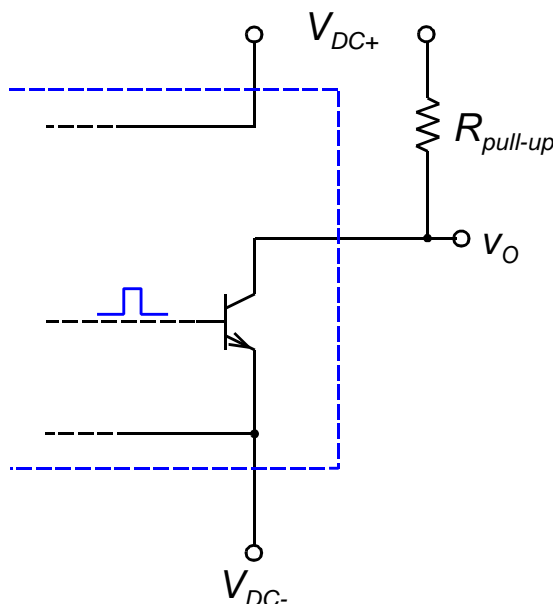


Fig. 144. Open-collector output.

An open-collector output uses a pull-up resistor instead of an active device.

Advantages are::

User-selected R , V_{DC} , and V_{OH}

$$V_{OL} \approx V_{CE \text{ sat}}$$

“Hot” element off chip

Wired NOR gate possible

But V_{OH} varies with load, and the circuit will be slow if $\tau = R_L C_L$ is large.

Schmitt Triggers

A Schmitt Trigger is a comparator with positive feedback, which provides hysteresis in the transfer characteristic. This solves the oscillation problem and provides noise immunity.

Inverting Schmitt Trigger:

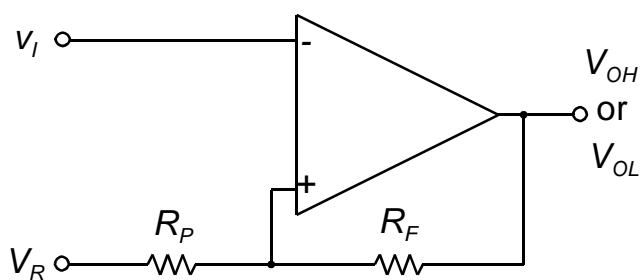


Fig. 146. Inverting Schmitt trigger.

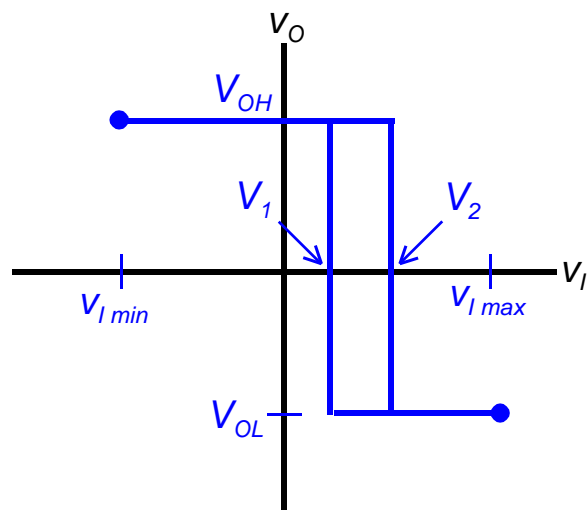


Fig. 145. Transfer function for inverting Schmitt trigger.

This is just a comparator with $V_{REF} = v^+$, the voltage at the noninverting input. Note that V_{REF} depends on V_R and v_O .

Switching occurs when $v_I = v^+$. For $v_O = V_{OH}$:

$$v^+ = \frac{V_R R_F + V_{OH} R_P}{R_F + R_P} = V_2 \quad (166)$$

and, for $v_O = V_{OL}$:

$$v^+ = \frac{V_R R_F + V_{OL} R_P}{R_F + R_P} = V_1 \quad (167)$$

From eqs. (166) and (167), we define the hysteresis voltage, V_H :

$$V_H = V_2 - V_1 = (V_{OH} - V_{OL}) \frac{R_P}{R_F + R_P} \quad (168)$$

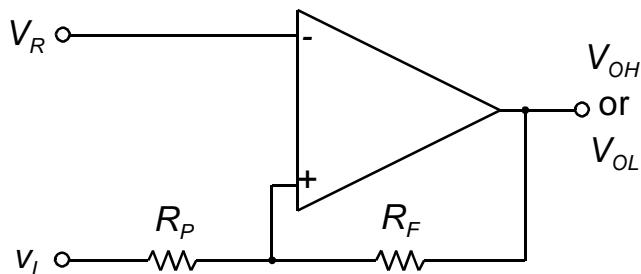
Noninverting Schmitt Trigger:

Fig. 147. Noninverting Schmitt trigger.

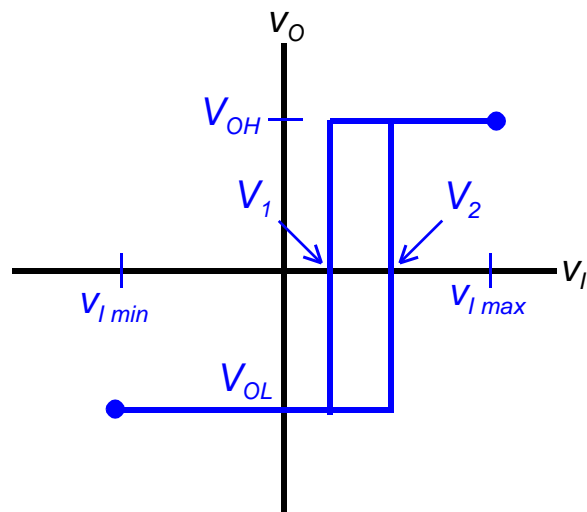


Fig. 148. Transfer function for noninverting Schmitt trigger.

Again, we have a comparator, but now v^+ depends on v_I and v_O .

For $v_O = V_{OH}$, let $v_I = V_1$ at the state change (i.e., when $v^+ = V_R$):

$$v^+ = V_R = \frac{V_1 R_F + V_{OH} R_P}{R_F + R_P} \Rightarrow V_1 = \frac{V_R (R_F + R_P) - V_{OH} R_P}{R_F} \quad (169)$$

And, for $v_O = V_{OL}$, let $v_I = V_2$ at the state change (when $v^+ = V_R$):

$$v^+ = V_R = \frac{V_2 R_F + V_{OL} R_P}{R_F + R_P} \Rightarrow V_2 = \frac{V_R (R_F + R_P) - V_{OL} R_P}{R_F} \quad (170)$$

In this case, the *hysteresis voltage*, V_H , is

$$V_H = V_2 - V_1 = (V_{OH} - V_{OL}) \frac{R_P}{R_F} \quad (171)$$

Schmitt Trigger Design:

To avoid oscillation for slowly changing inputs, only a few mV of hysteresis voltage is usually required.

This means that $R_P \ll R_F$. A very approximate typical ratio for these resistors is 1:100.

For $R_P \ll R_F$ eq. (168) becomes nearly equal to (171), and hysteresis voltage for either the noninverting or the inverting Schmitt trigger is given by:

$$V_H \approx (V_{OH} - V_{OL}) \frac{R_P}{R_F} \quad (172)$$

To aid your understanding of Schmitt triggers, remember these two key points:

1. Switching level depends on the state of the output
 2. The feedback is always positive, regardless of the connection used.
-

Schmitt Trigger Example:

A comparator with a totem-pole output operates from a single 12 V supply with $V_{OH} = 10\text{ V}$ and $V_{OL} = 0$.

Design an *inverting Schmitt trigger* that switches at 2V and 6V.

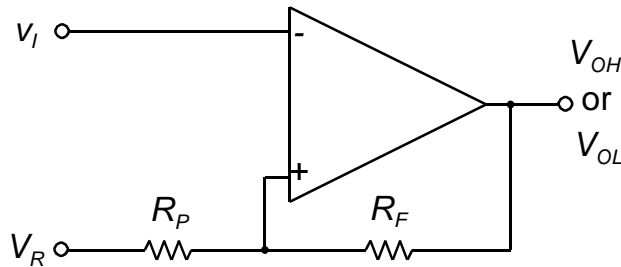


Fig. 149. Inverting Schmitt trigger of example.

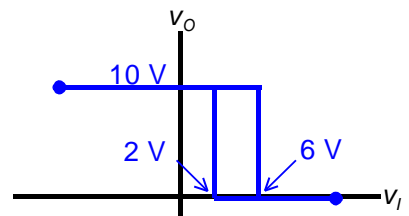


Fig. 150. Transfer function for example.

When $v_O = 0$ we want switching at $v_I = 2\text{ V}$:

$$V_1 = 2\text{ V} = V_R \frac{R_F}{R_F + R_P} \quad (173)$$

When $v_O = 10$ we want switching at $v_I = 6\text{ V}$:

$$V_2 = 6\text{ V} = \frac{V_R R_F + 10 R_P}{R_F + R_P} \quad (174)$$

Now, $V_2 - V_1 = V_H$:

$$V_H = \frac{V_R R_F + 10 R_P}{R_F + R_P} - \frac{V_R R_F}{R_F + R_P} = \frac{10 R_P}{R_F + R_P} = 4\text{ V} \quad (175)$$

Note we have only one equation, but two unknowns . . . we get to arbitrarily choose one of the unknowns!!!

We may select R_F , R_P , or $R_F + R_P$. . . we'll let $R_F + R_P = 100 \text{ k}\Omega$.

Then, from eq. (175), $10R_P = 400 \text{ k}\Omega$, thus:

$$R_P = 40 \text{ k}\Omega \quad \text{and} \quad R_F = 60 \text{ k}\Omega \quad (176)$$

Finally, we can use either (173) or (174) to solve for V_R .

From (173) (it's the easier one!):

$$V_R = 2 \text{ V} \frac{R_F + R_P}{R_F} = 3.33 \text{ V} \quad (177)$$

We already have a 12 V supply, so we obtain V_R and R_P with a voltage divider from that supply:

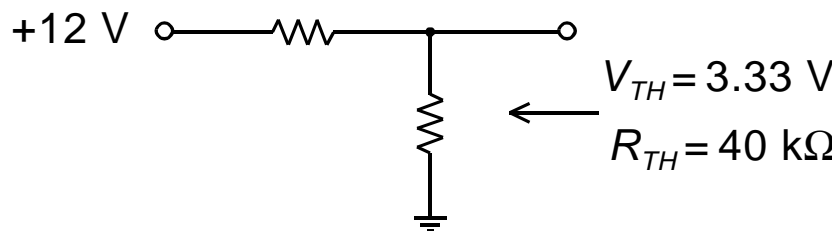
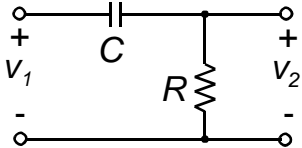
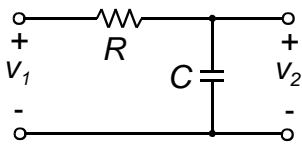
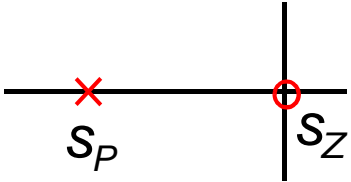
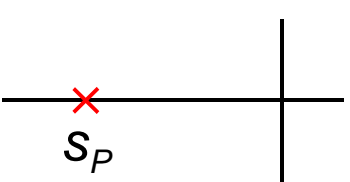
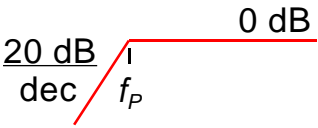
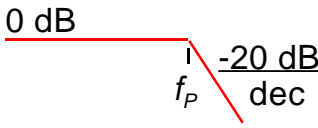
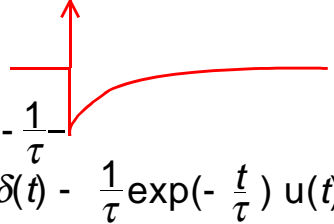
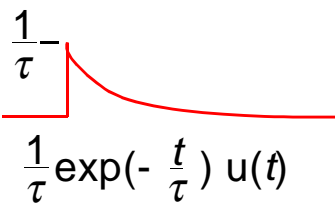


Fig. 151. Using a voltage divider to obtain V_R and R_P .

The details of the calculations implied by Fig. 151 are left for you to work out . . .

Single-Pole Circuits

Example	 <p>Fig. 152. High Pass</p>	 <p>Fig. 153. Low Pass</p>
Time Constant	$\tau = RC$ or $\tau = L/R$	
Transfer Function $T(s) = \frac{V_2(s)}{V_1(s)}$	$T(s) = \frac{s}{s + \frac{1}{\tau}}$	$T(s) = \frac{1}{\tau \left(s + \frac{1}{\tau} \right)}$
Pole-Zero Pattern $s_p = -1/\tau$	 <p>Fig. 154. HP pole-zeros.</p>	 <p>Fig. 155. LP pole-zeros.</p>
Bode Magnitude Plot $\omega_p = 1/\tau$	 <p>Fig. 156. HP Bode plot.</p>	 <p>Fig. 157. LP Bode plot.</p>
Impulse Response $v_2(t)$	 <p>Fig. 158. HP impulse resp</p>	 <p>Fig. 159. LP impulse resp</p>
Natural Response	$v_2(t) = (1/\tau) \exp(-t/\tau) u(t)$	
Differential Eq.	$v_2' + (1/\tau)v_2 = v_1'$	$v_2' + (1/\tau)v_2 = v_1/\tau$

General Response to Piecewise-Constant Inputs

In any single-pole circuit, within any interval in which the input is constant, the response will always have the form:

$$r(t) = A + B \exp\left(-\frac{t}{\tau}\right), \quad t_{\text{start}} < t < t_{\text{end}} \quad (178)$$

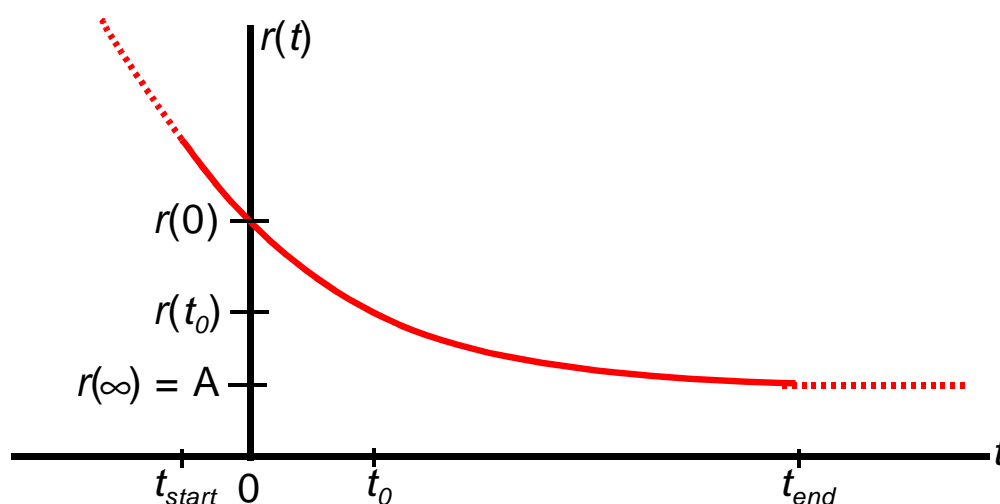


Fig. 160. General exponential (single-pole) response.

The time constant τ is usually known or can be determined from the circuit. The remaining unknowns in eq. (178) are the coefficients A and B , so we need to know the value of $r(t)$ at two points.

Usually $r(\infty)$ can be determined by inspection . . . and from eq. (178) with $t = \infty$, we have:

$$A = r(\infty) \quad (179)$$

This is already noted on the $r(t)$ axis in Fig. 160.

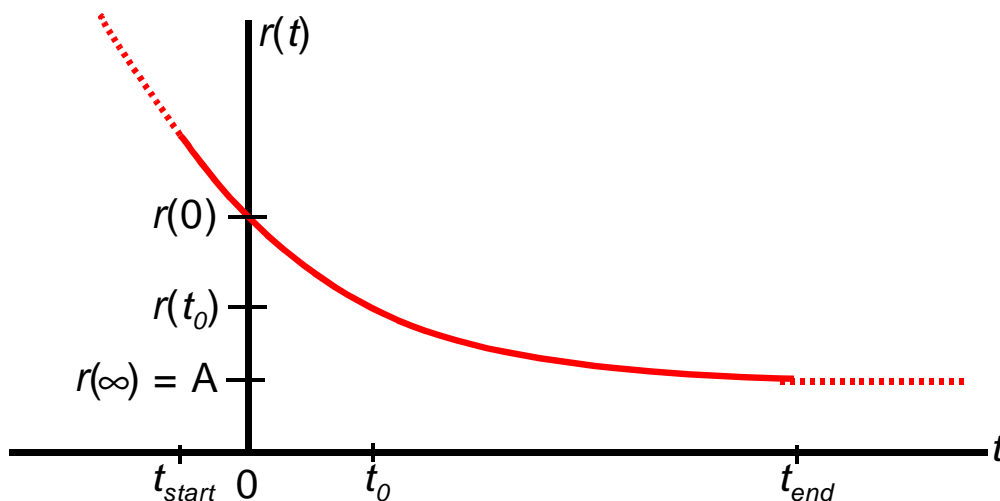


Fig. 161. General exponential response (Fig. 160 repeated).

We can also write:

$$r(0) = A + B \exp(0) = A + B \quad (180)$$

which is mathematically valid even if $r(0)$ is not within the interval. Often, though $r(0)$ is not only within the interval, but it is the start of the interval. In either case:

$$B = r(0) - A = r(0) - r(\infty) \quad (181)$$

So we can write the general response expression in the form:

$$r(t) = r(\infty) + [r(0) - r(\infty)] \exp\left(-\frac{t}{\tau}\right) \quad (182)$$

Similarly, if the response $r(t)$ is known at $t = t_0$ rather than at $t = 0$, eq. (182) becomes:

$$r(t) = r(\infty) + [r(t_0) - r(\infty)] \exp\left[\frac{-(t - t_0)}{\tau}\right] \quad (183)$$

Time Interval Between Known Values of Exponential Response

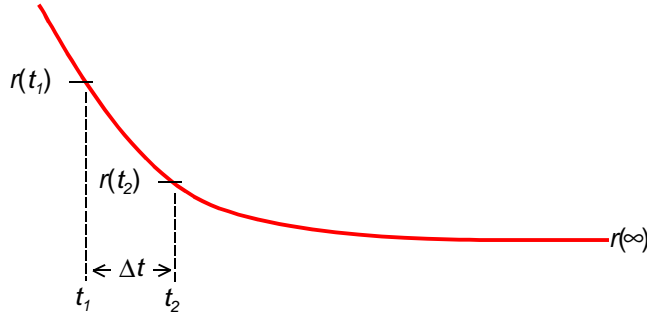


Fig. 162. General exponential response.

Given:

$$\tau, r(t_1), r(t_2), r(\infty)$$

i.e., the function is known at three points.

We wish to determine an expression for the interval Δt .

We know $r(t_1)$, so we'll let it serve as the time reference point for the general response equation (183):

$$r(t) = r(\infty) + [r(t_1) - r(\infty)] \exp\left[\frac{-(t - t_1)}{\tau}\right] \quad (184)$$

Then, at t_2 :

$$r(t_2) = r(\infty) + [r(t_1) - r(\infty)] \exp\left[\frac{-(t_2 - t_1)}{\tau}\right] \quad (185)$$

Now we solve eq. (185) for $t_2 - t_1$, which is the interval Δt of interest:

$$\frac{r(t_2) - r(\infty)}{r(t_1) - r(\infty)} = \exp\left[\frac{-(t_2 - t_1)}{\tau}\right] = \exp\left(\frac{-\Delta t}{\tau}\right) \quad (186)$$

For notational convenience, we let

$$p = \frac{r(t_2) - r(\infty)}{r(t_1) - r(\infty)} = \frac{\text{total change in } r \text{ after } t_2}{\text{total change in } r \text{ after } t_1} \quad (187)$$

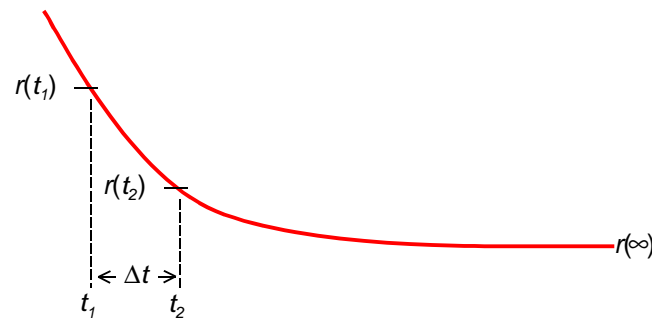


Fig. 163. General exponential response (Fig. 162 repeated).

Continuing with our derivation, we have:

$$p = \exp\left(\frac{-\Delta t}{\tau}\right) \Rightarrow \frac{1}{p} = \exp\left(\frac{\Delta t}{\tau}\right) \quad (188)$$

From which:

$$\Delta t = \tau \ln\left(\frac{1}{p}\right) \quad (189)$$

Example:

A power supply filter capacitor of $10,000 \mu\text{F}$ is in parallel with a 50Ω load in a 10 V system. How long will it take for the load voltage to drop to 7.5 V after the supply is turned off?

Solution:

$$\tau = RC = 0.5 \text{ s} \quad p = \frac{7.5 \text{ V}}{10 \text{ V}} = \frac{3}{4} \quad (190)$$

$$\Delta t = 0.5 \ln\left(\frac{4}{3}\right) = 144 \text{ ms}$$

Pulse Response of Single-Pole High-Pass

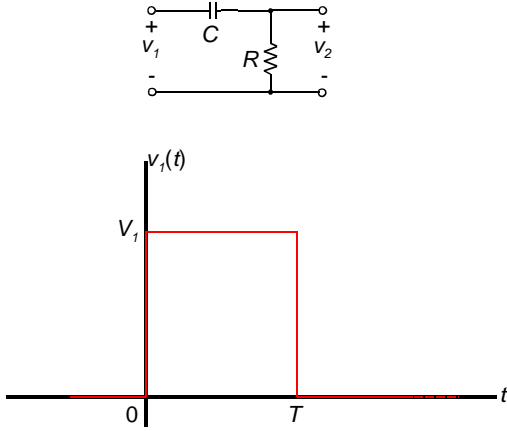


Fig. 164. High-pass filter and input pulse.

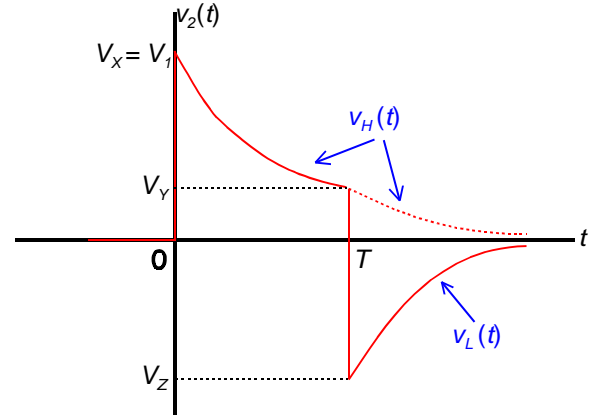


Fig. 165. Pulse response of HPF.

Assume $v_1(t) = 0$ for $t < 0$. . . then $v_2(t) = 0$ for $t < 0$ also.

For $t = 0$:

Capacitor voltage cannot change instantaneously without a current impulse, which would require infinite source voltage, thus:

$$\Delta v_1 = \Delta v_2 = V_1 \quad \Rightarrow \quad V_x = V_1 \quad (191)$$

For $0 < t < T$:

We have a piecewise-constant input, thus:

$$v_H(t) = v_H(\infty) + [v_H(t_0) - v_H(\infty)] \exp\left[-\frac{t-t_0}{\tau}\right] \quad (192)$$

where

$$v_H(\infty) = 0, \quad t_0 = 0, \quad \text{and} \quad v_H(t_0) = V_1 \quad (193)$$

from which:

$$v_2(t) = V_1 \exp\left(-\frac{t}{\tau}\right), \quad 0 < t < T \quad (194)$$

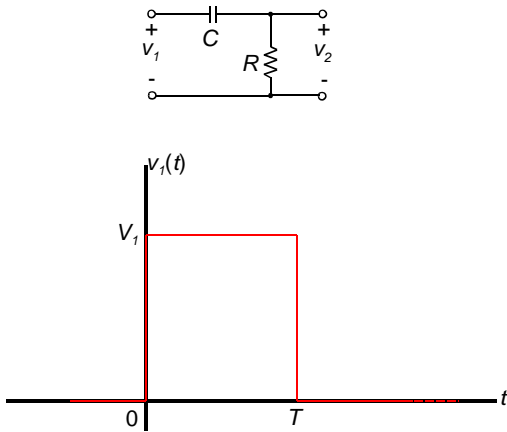


Fig. 166. High-pass filter and input pulse (Fig. 164 repeated).

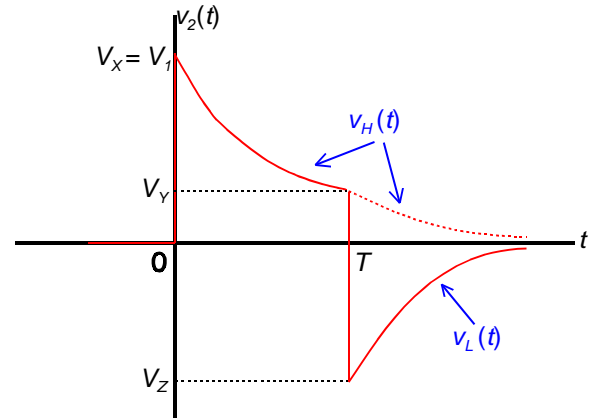


Fig. 167. Pulse response of HPF (Fig. 165, 171 repeated).

Note from eq. (194) that at $t = T^-$:

$$v_2(T^-) = V_1 \exp\left(-\frac{T}{\tau}\right) = V_Y \quad (195)$$

For $t = T$:

Again $\Delta v_1 = \Delta v_2 = V_1$, and:

$$V_Z = V_Y - V_1 = V_1 \exp\left(-\frac{T}{\tau}\right) - V_1 = V_1 \left[\exp\left(-\frac{T}{\tau}\right) - 1 \right] \quad (196)$$

For $T < t < \infty$:

We again have piecewise-constant input, thus:

$$v_L(t) = v_L(\infty) + [v_L(t_0) - v_L(\infty)] \exp\left[-\frac{t-t_0}{\tau}\right] \quad (197)$$

where

$$v_L(\infty) = 0, \quad t_0 = T, \quad \text{and} \quad v_L(T) = V_Z \quad (198)$$

from which

$$v_2(t) = V_Z \exp\left(-\frac{t-T}{\tau}\right), \quad t > T \quad (199)$$

Pulse Response of Single-Pole Low-Pass

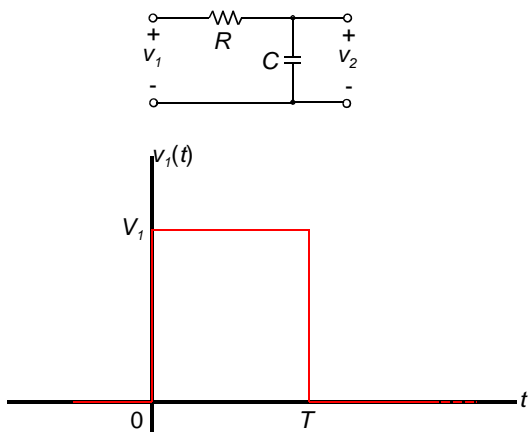


Fig. 168. Low-pass filter and input pulse.

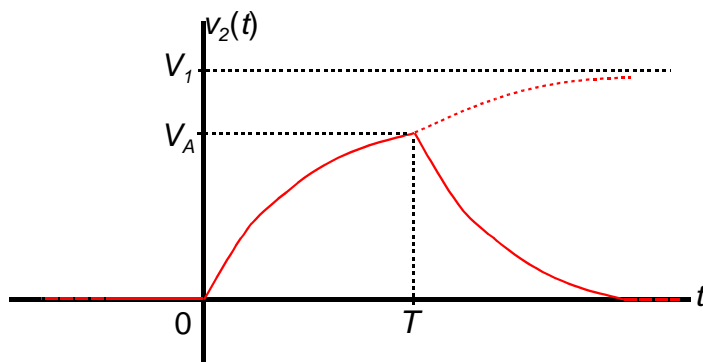


Fig. 169. Pulse response of LPF.

Assume $v_1(t) = 0$ for $t < 0$. . . then $v_2(t) = 0$ for $t < 0$ also.

At $t = 0$:

Capacitor voltage cannot change instantaneously without a current impulse, which would require infinite source voltage, thus:

$$v_2(0^+) = 0 \quad (200)$$

For $0 < t < T$:

We have a piecewise-constant input, thus:

$$v_H(t) = v_H(\infty) + [v_H(t_0) - v_H(\infty)] \exp\left[-\frac{t-t_0}{\tau}\right] \quad (201)$$

where:

$$v_H(\infty) = V_1, \quad t_0 = 0, \quad \text{and} \quad v_H(t_0) = 0 \quad (202)$$

from which:

$$v_2(t) = V_1 \left[1 - \exp\left(-\frac{t}{\tau}\right) \right], \quad 0 < t < T \quad (203)$$

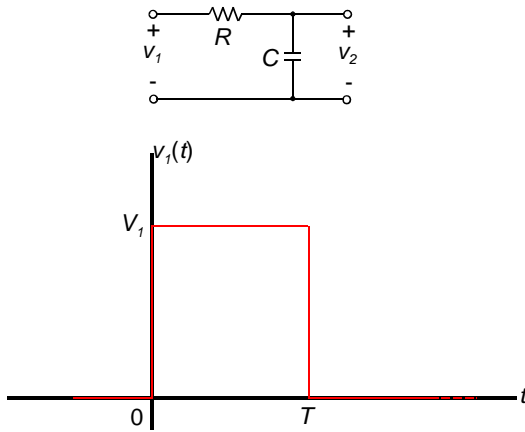


Fig. 170. Low-pass filter and input pulse (Fig. 168 repeated).

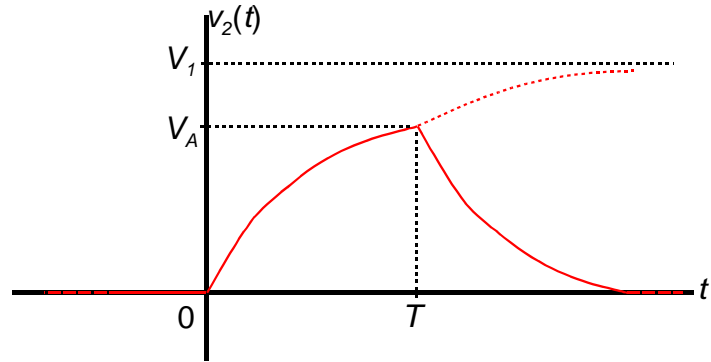


Fig. 171. Pulse response of LPF (Fig. 169 repeated).

Note from eq. (203) that at $t = T^-$:

$$v_2(T^-) = V_1 \left[1 - \exp\left(-\frac{T}{\tau}\right) \right] = V_A \quad (204)$$

At $t = T^+$:

Again, because $\Delta v_{\text{capacitor}} = 0$:

$$v_2(T^+) = v_2(T^-) = V_A \quad (205)$$

For $T < t < \infty$:

We again have piecewise-constant input, thus:

$$v_L(t) = v_L(\infty) + [v_L(t_0) - v_L(\infty)] \exp\left[-\frac{t-t_0}{\tau}\right] \quad (206)$$

where:

$$v_L(\infty) = 0, \quad t_0 = T, \quad \text{and} \quad v_L(T) = V_A \quad (207)$$

from which:

$$v_2(t) = V_A \exp\left(-\frac{t-T}{\tau}\right) = V_1 \left[1 - \exp\left(-\frac{T}{\tau}\right) \right] \exp\left(-\frac{t-T}{\tau}\right), \quad t > T \quad (208)$$

Steady-State Rectangular-Wave Response of Single-Pole High-Pass

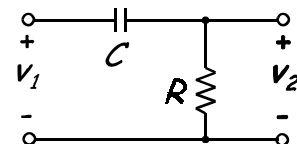


Fig. 172. High pass

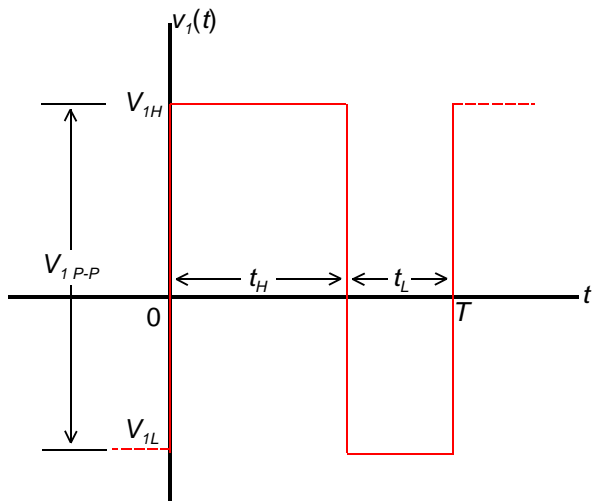


Fig. 173. Rectangular wave input.

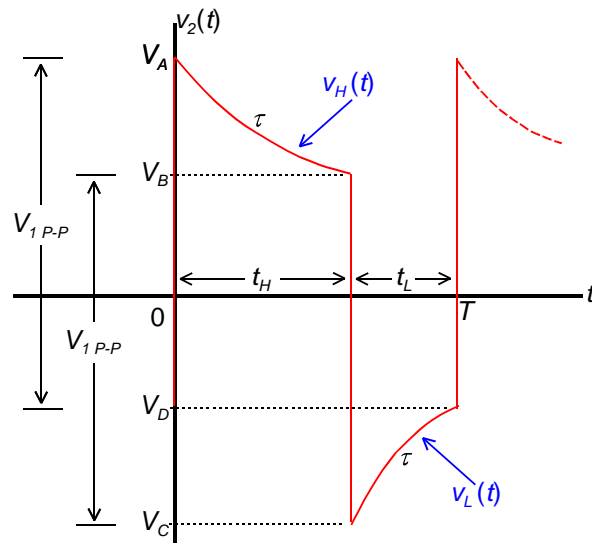


Fig. 174. Steady-state HP response.

- Key Ideas:
1. v_2 has zero dc component.
 2. Capacitor voltage can't change instantly
 $\therefore V_A - V_D = V_{1 P-P} = V_B - V_C$.
 3. $v_H(\infty) = 0 = v_L(\infty)$.
 4. Steady-State \Rightarrow Natural response has died.
 5. Each cycle is identical to the preceding one.

- Approach:
1. Assume arbitrary initial value V_A .
 2. Calculate response waveform through a full cycle.
 3. Set value at end of period to initial value V_A .

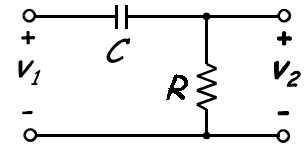


Fig. 175. High pass

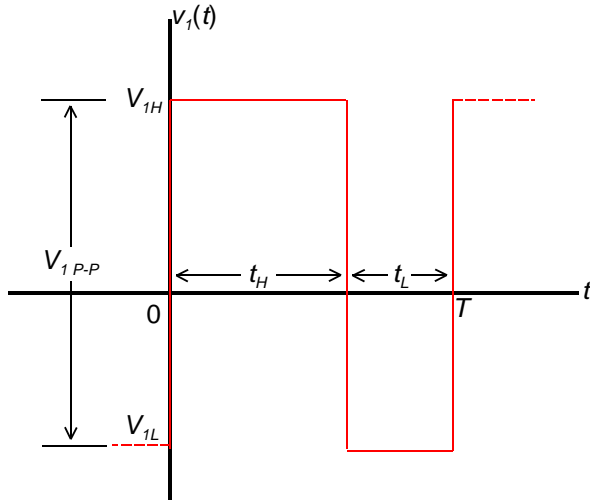


Fig. 176. Rectangular wave input (Fig. 173 repeated).

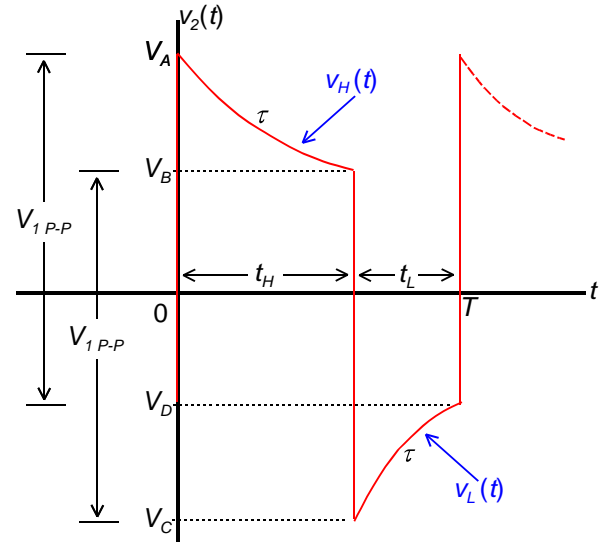


Fig. 177. Steady-state HP response (Fig. 174 repeated).

To calculate the response waveform through a full cycle, we'll begin with the general response to a piecewise-constant input:

$$r(t) = r(\infty) + [r(t_0) - r(\infty)] \exp\left[\frac{-(t - t_0)}{\tau}\right] \quad (209)$$

For $0 < t < t_H$:

$$v_H(t) = V_A \exp\left(-\frac{t}{\tau}\right) \quad (210)$$

For $t_H^- < t < t_H^+$:

$$V_B = v_H(t_H^-) = V_A \exp\left(-\frac{t_H}{\tau}\right) \quad (211)$$

and

$$V_C = V_B - V_{1P-P} = V_A \exp\left(-\frac{t_H}{\tau}\right) - V_{1P-P} \quad (212)$$

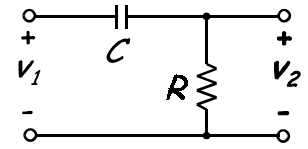


Fig. 178. High pass

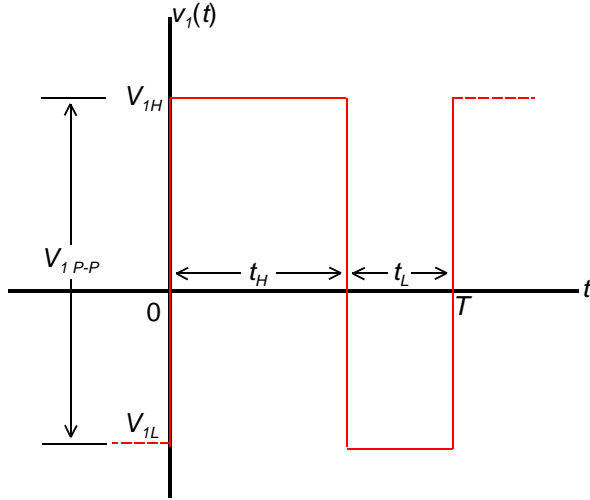


Fig. 179. Rectangular wave input (Fig. 173 repeated).

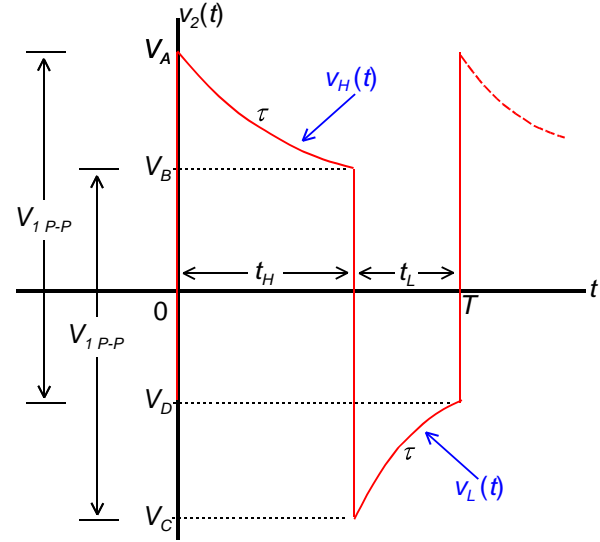


Fig. 180. Steady-state HP response (Fig. 174 repeated).

For $t_H < t < T$:

$$v_L(t) = V_C \exp\left(-\frac{t - t_H}{\tau}\right) \quad (213)$$

For $T^- < t < T^+$:

$$\begin{aligned} V_D = v_L(T) &= V_C \exp\left(-\frac{T - t_H}{\tau}\right) \\ &= \left[V_A \exp\left(-\frac{t_H}{\tau}\right) - V_{1P-P} \right] \exp\left(-\frac{t_L}{\tau}\right) \end{aligned} \quad (214)$$

And, finally:

$$v_2(T^+) = V_A = V_D + V_{1P-P} \quad (215)$$

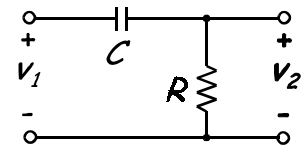


Fig. 181. High pass

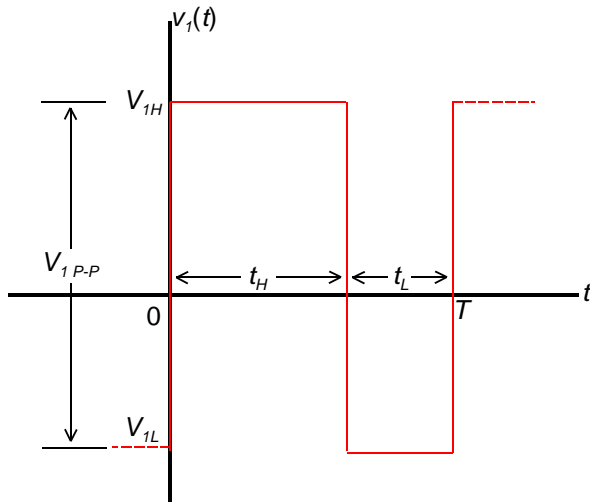


Fig. 182. Rectangular wave input (Fig. 173 repeated).

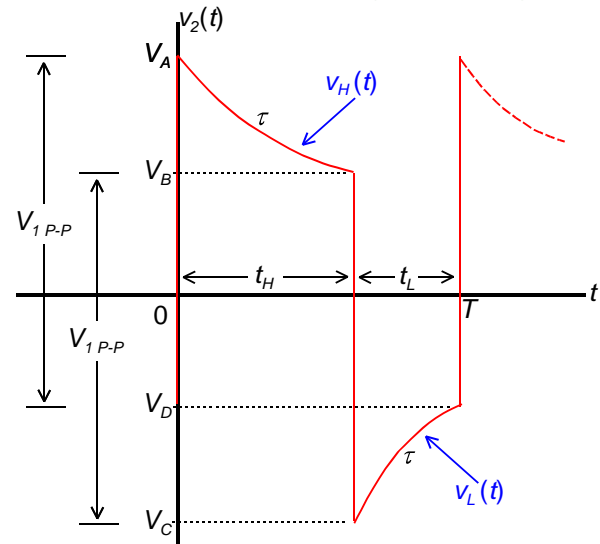


Fig. 183. Steady-state HP response (Fig. 174 repeated).

Now, we re-write eq. (215) using the expression for V_D from eq. (214):

$$V_A = \left[V_A \exp\left(-\frac{t_H}{\tau}\right) - V_{1P-P} \right] \exp\left(-\frac{t_L}{\tau}\right) + V_{1P-P} \quad (216)$$

Rearranging:

$$V_A - V_A \exp\left(-\frac{t_H}{\tau}\right) \exp\left(-\frac{t_L}{\tau}\right) = V_{1P-P} - V_{1P-P} \exp\left(-\frac{t_L}{\tau}\right) \quad (217)$$

And finally solving for V_A :

$$V_A = \frac{V_{1P-P} \left[1 - \exp\left(-\frac{t_L}{\tau}\right) \right]}{\left[1 - \exp\left(-\frac{T}{\tau}\right) \right]} \quad (218)$$

With V_A determined we can find V_B , V_C , and V_D by going back through the derived equations.

Special Cases:

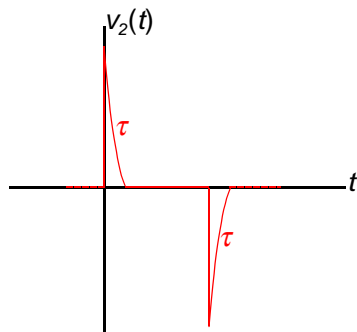


Fig. 184. HP Steady-state rectangular-wave response, for small τ .

1. For $\tau \ll t_H, t_L$:

We will have $V_B \approx 0$, $V_D \approx 0$,
and $V_{2\text{ P-P}} \approx 2 V_{1\text{ P-P}}$.

In this case the circuit is known as a differentiator.

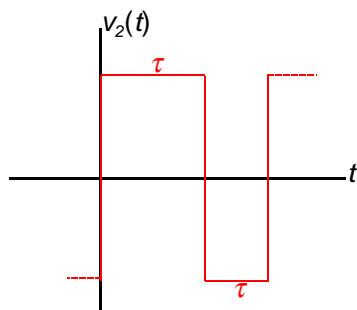


Fig. 185. HP Steady-state rectangular-wave response, for large τ .

2. For $\tau \gg t_H, t_L$,

We will have $V_B \approx V_A$ and $V_D \approx V_C$,
and $V_{2\text{ P-P}} \approx V_{1\text{ P-P}}$.

In this case the output is just input with dc removed!!!

3. For any square wave input, $t_H = t_L = T/2$,

The output must still have zero average, so waveform must be symmetrical around the t axis, i.e., $V_C = -V_A$ and $V_D = -V_B$.

Steady-State Rectangular-Wave Response of Single-Pole Low-Pass

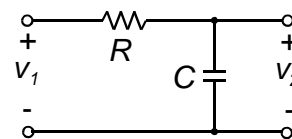


Fig. 186. Low pass.

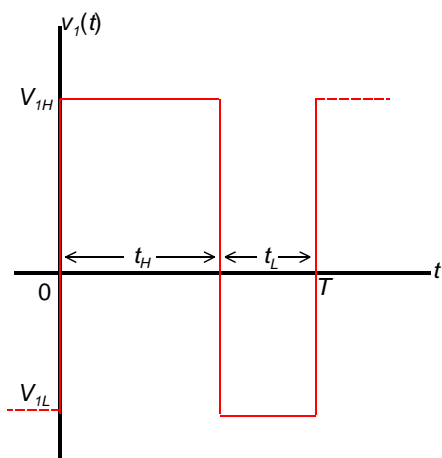


Fig. 187. Rectangular wave input.

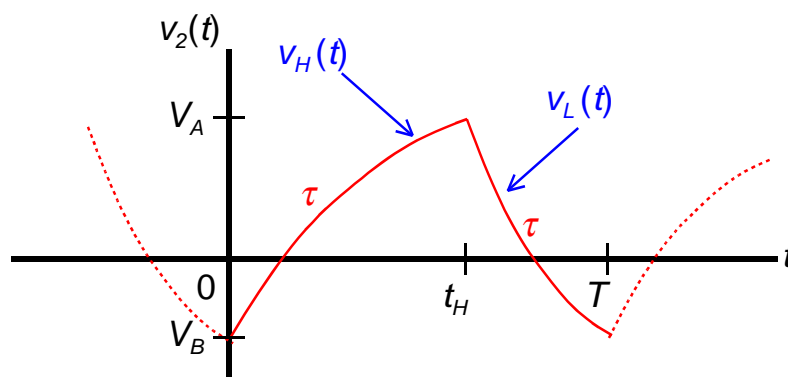


Fig. 188. Steady-state LP response.

- Key Ideas:
1. Average of v_2 = average of v_1 (same dc component)
 2. $v_H(\infty) = V_{1H}$ and $v_L(\infty) = V_{1L}$.
 3. Steady-State \Rightarrow Natural response has died.
 4. Each cycle is identical to the preceding one.

- Approach:
1. Assume arbitrary initial value.
 2. Calculate response waveform through a full cycle.
 3. Set value at end of period to initial value.

We begin with the general response to a piecewise-constant input:

$$r(t) = r(\infty) + [r(t_0) - r(\infty)] \exp\left[\frac{-(t - t_0)}{\tau}\right] \quad (219)$$

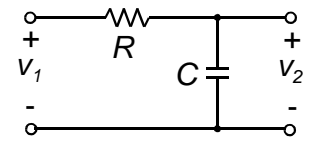


Fig. 189. Low pass.

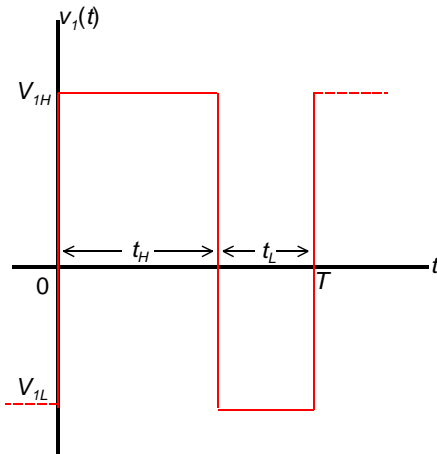
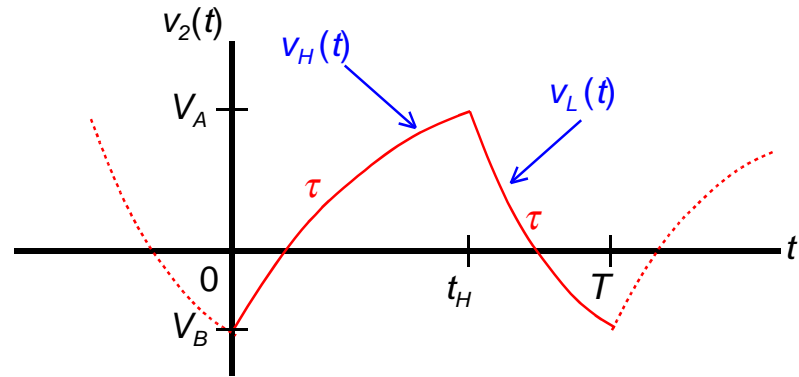
Fig. 190. Rectangular wave input
(Fig. 187 repeated).

Fig. 191. Steady-state LP response (Fig. 188 repeated).

For $0 \leq t \leq t_H$:

$$v_H(t) = V_{1H} + [V_B - V_{1H}] \exp\left(-\frac{t}{\tau}\right) \quad (220)$$

At $t = t_H$:

$$\begin{aligned} V_A &= V_{1H} + [V_B - V_{1H}] \exp\left(-\frac{t_H}{\tau}\right) \\ &= V_{1H} \left[1 - \exp\left(-\frac{t_H}{\tau}\right)\right] + V_B \exp\left(-\frac{t_H}{\tau}\right) \end{aligned} \quad (221)$$

For $t_H \leq t \leq T$:

$$v_L(t) = V_{1L} + [V_A - V_{1L}] \exp\left(-\frac{t - t_H}{\tau}\right) \quad (222)$$

At $t = T$:

$$V_B = V_{1L} + [V_A - V_{1L}] \exp\left(-\frac{T - t_H}{\tau}\right) \quad (223)$$

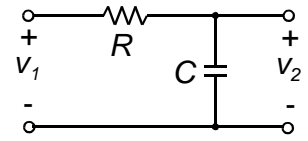


Fig. 192. Low pass.

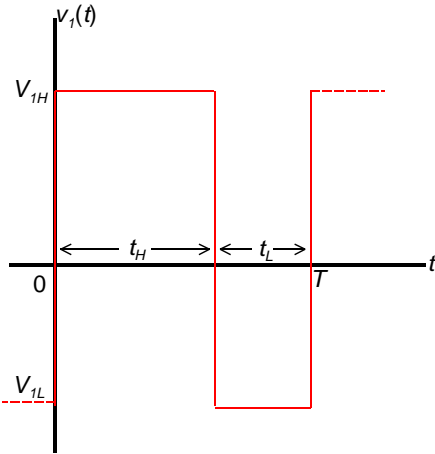
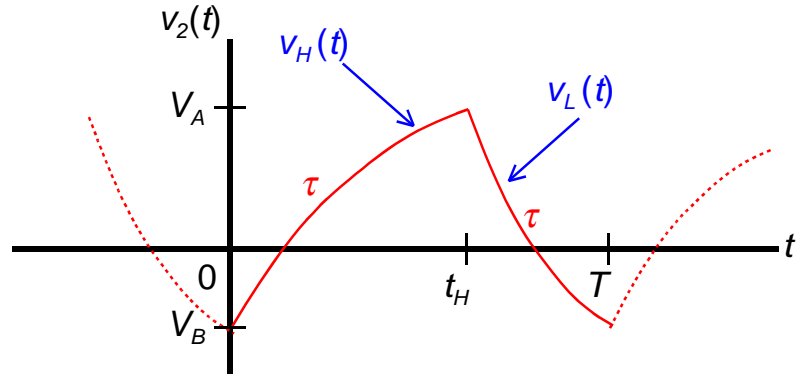
Fig. 193. Rectangular wave input
(Fig. 187 repeated).

Fig. 194. Steady-state LP response (Fig. 188 repeated).

Continuing at $t = T$, we re-write eq.(223):

$$V_B = V_{1L} \left[1 - \exp\left(-\frac{t_L}{\tau}\right) \right] + V_A \exp\left(-\frac{t_L}{\tau}\right) \quad (224)$$

Now we use the above equation to substitute for V_B in eq. (221):

$$\begin{aligned} V_A = & V_{1H} \left[1 - \exp\left(-\frac{t_H}{\tau}\right) \right] + V_{1L} \left[1 - \exp\left(-\frac{t_L}{\tau}\right) \right] \exp\left(-\frac{t_H}{\tau}\right) \dots \\ & \dots + V_A \exp\left(-\frac{t_L}{\tau}\right) \exp\left(-\frac{t_H}{\tau}\right) \end{aligned} \quad (225)$$

Rearranging:

$$\begin{aligned} V_A \left[1 - \exp\left(-\frac{T}{\tau}\right) \right] = & \dots \\ \dots V_{1H} \left[1 - \exp\left(-\frac{t_H}{\tau}\right) \right] + V_{1L} \exp\left(-\frac{t_H}{\tau}\right) \left[1 - \exp\left(-\frac{t_L}{\tau}\right) \right] \end{aligned} \quad (226)$$

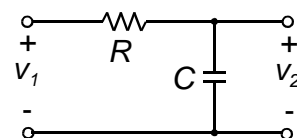


Fig. 195. Low pass.

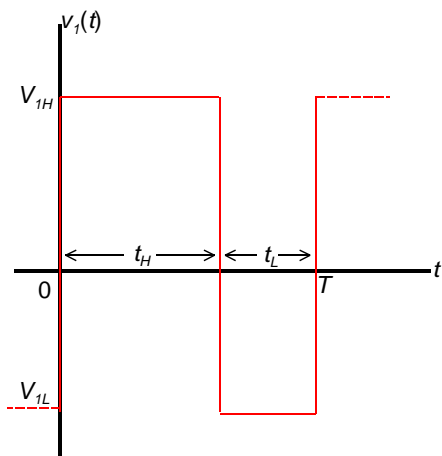
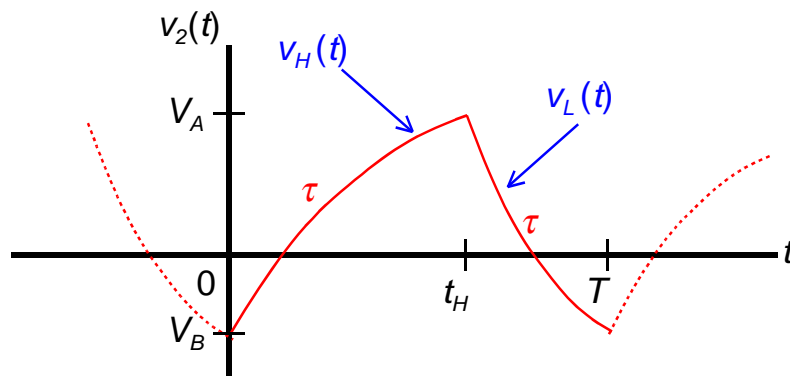
Fig. 196. Rectangular wave input
(Fig. 187 repeated).

Fig. 197. Steady-state LP response (Fig. 188 repeated).

Finally, we solve eq. (226) for V_A :

$$V_A = \frac{V_{1H} \left[1 - \exp\left(-\frac{t_H}{\tau}\right) \right] + V_{1L} \exp\left(-\frac{t_H}{\tau}\right) \left[1 - \exp\left(-\frac{t_L}{\tau}\right) \right]}{1 - \exp\left(-\frac{T}{\tau}\right)} \quad (227)$$

In similar fashion, we could have used eq. (221) to substitute for V_A in eq. (224), and solved for V_B :

$$V_B = \frac{V_{1L} \left[1 - \exp\left(-\frac{t_L}{\tau}\right) \right] + V_{1H} \exp\left(-\frac{t_L}{\tau}\right) \left[1 - \exp\left(-\frac{t_H}{\tau}\right) \right]}{1 - \exp\left(-\frac{T}{\tau}\right)} \quad (228)$$

555 IC Precision Timer

Introduction

The 555 is an integrated circuit that performs the basic function of a precision timer. Other functions and features are:

- Astable multivibrator, monostable multivibrator, pulse width modulator, pulse position modulator, *many* other applications.
 - Timing from microseconds to hours!!!
 - Timing determined by resistor ratios - independent of V_{CC} .
 - Operating frequency up to 500 kHz.
 - Wide supply voltage range - 4.5 V to 18 V.
 - Compatible with TTL and CMOS logic.
 - Totem-pole output.
 - Output can source or sink 200 mA.
 - Can be reset (i.e., gated, or disabled).
-

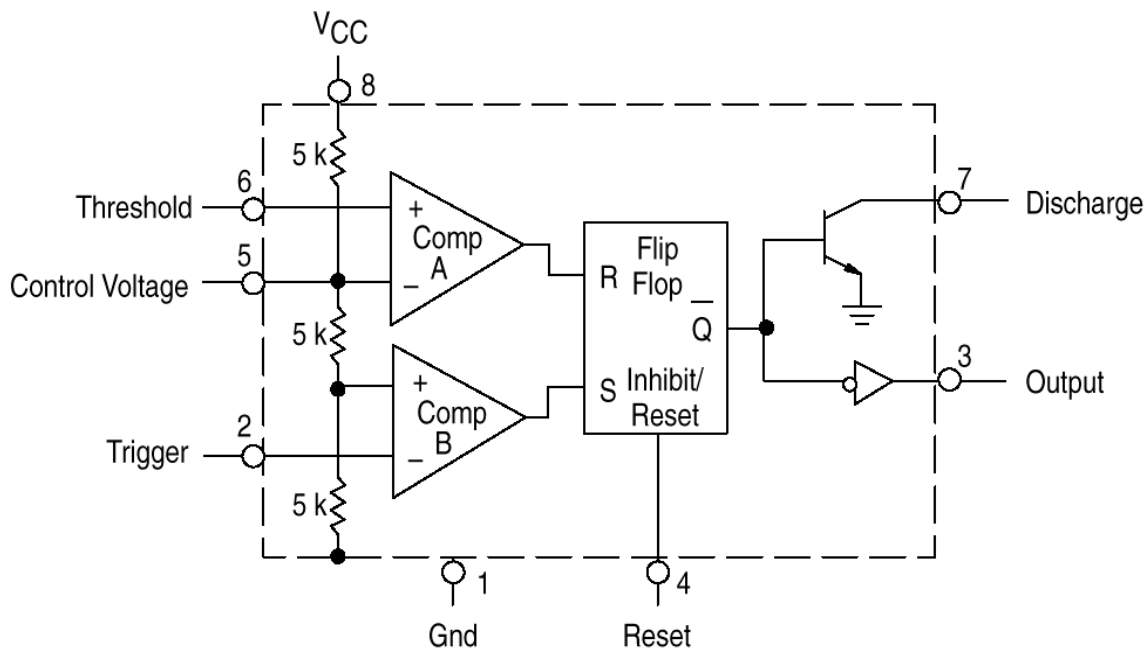


Fig. 198. Function diagram of 555 timer, from Motorola's MC1455 data sheet, available via www.motorola.com.

The functional diagram of a 555 timer is shown above. Note the following characteristics from the diagram.

Inputs:

V_{TH} , threshold voltage.

V_{CV} , control voltage.

V_{TR} , trigger voltage.

V_R , reset voltage.

RS flip-flop:

When **reset** (R input is high), Q output is low.

When **set** (S input is high), Q output is high.

Comparator reference voltages:

Threshold comparator ("Comp A"): $\frac{2}{3} V_{CC}$ or V_{CV}

Trigger Comparator ("Comp B"): $\frac{1}{3} V_{CC}$ or $\frac{1}{2} V_{CV}$

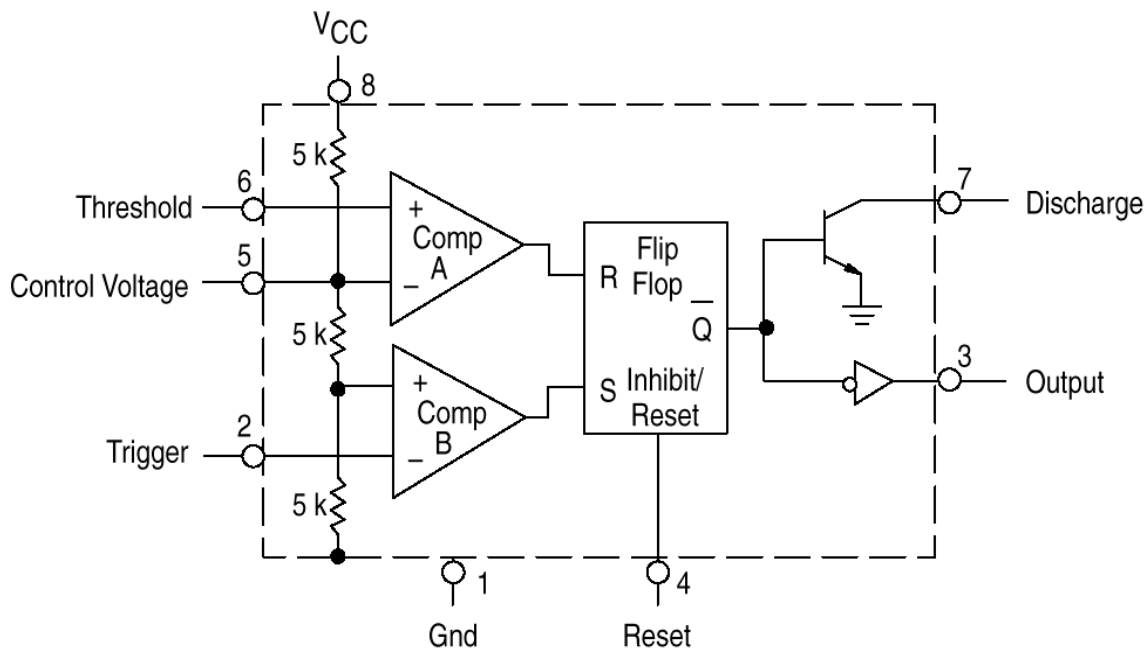


Fig. 199. Function diagram of 555 timer (Fig. 198 repeated).

Features of the threshold comparator:

“Active high” \Rightarrow when $V_{TH} > V_{CV}$

When active, the flip-flop is reset, $v_O = V_{OL}$, and the discharge transistor is on.

Features of the trigger comparator:

“Active low” \Rightarrow when $V_{TR} < V_{CV}/2$

When active, the flip-flop is set, $v_O = V_{OH}$, and the discharge transistor is .

Simultaneous active threshold and trigger comparators not allowed.

Features of the reset input:

Active low \Rightarrow when $V_R \ll V_{BE} (\approx 0.4 \text{ V})$

When active, the flip-flop is reset. The reset input overrides the flip-flop R and S inputs.

Monostable Multivibrator

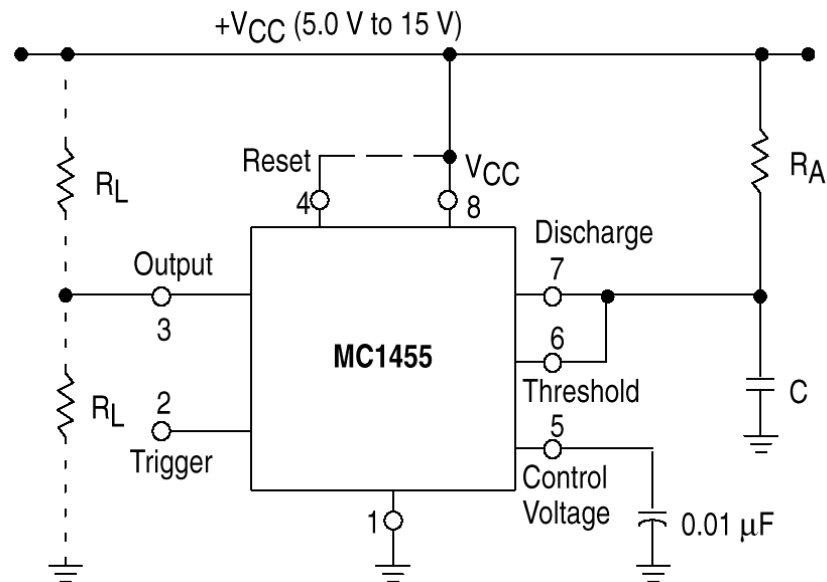


Fig. 200. Monostable MV using 555 timer.

The 555 monostable multivibrator, shown above, generates a single output pulse when the input is triggered.

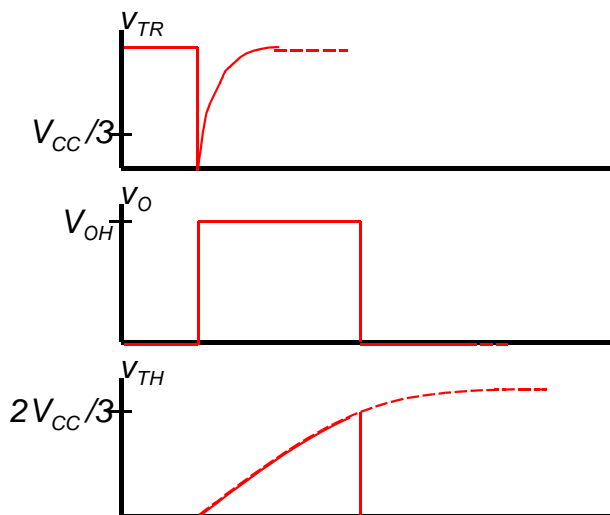


Fig. 201. Monostable MV waveforms.

Operation:

1. The circuit rests in its stable, **reset** state:

$$v_O = V_{OL}, \quad Q_{\text{discharge}} \text{ on}, \quad V_{TH} = 0$$

2. When the circuit receives a trigger pulse $\Rightarrow V_{TR} < V_{CC}/3$:

$$f\text{-}f \text{ is } \mathbf{set}, \quad v_O = V_{OH} \quad Q_{\text{discharge}} \text{ off}$$

C charges toward V_{CC}

3. When V_{TH} reaches $2V_{CC}/3$:

f-f **resets** to stable state

$$v_O = V_{OL}, \quad Q_{\text{discharge}} \text{ on}, \quad V_{TH} = 0$$

Calculating the Output Pulse Width:

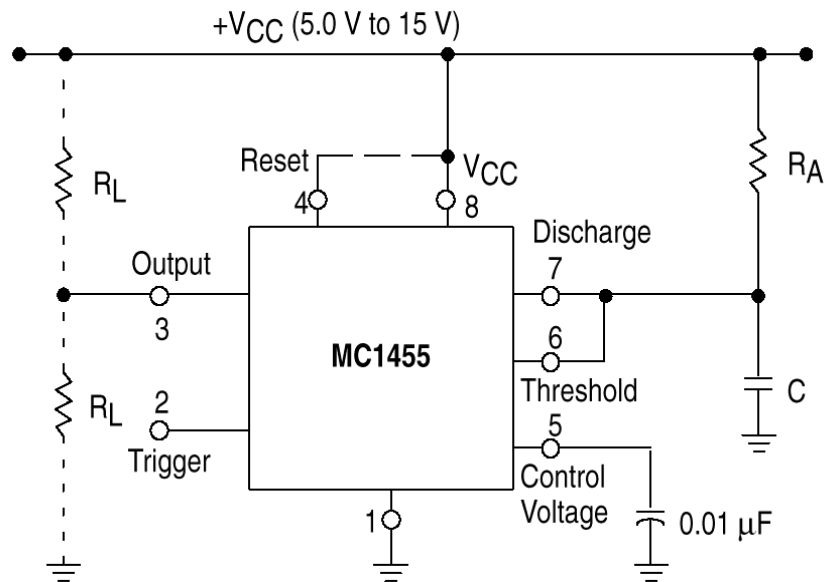


Fig. 202. Monostable MV using 555 timer (Fig. 200 repeated).

Once the circuit is triggered, C charges through R_A , with;

$$\tau = R_A C \quad (229)$$

Thus, the output pulse width will be:

$$T = \tau \ln \frac{1}{p} \quad (230)$$

where

$$p = \frac{V_{CC} - \frac{2}{3}V_{CC}}{V_{CC}} = \frac{1}{3} \quad (231)$$

Thus:

$$T = \tau \ln 3 = 1.10\tau \quad (232)$$

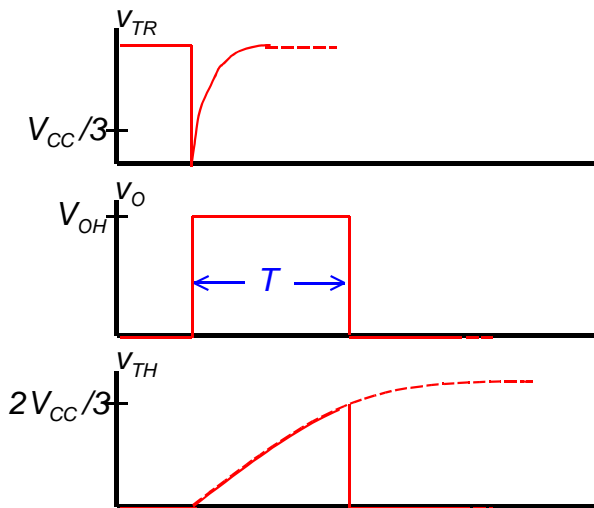


Fig. 203. Monostable waveforms.

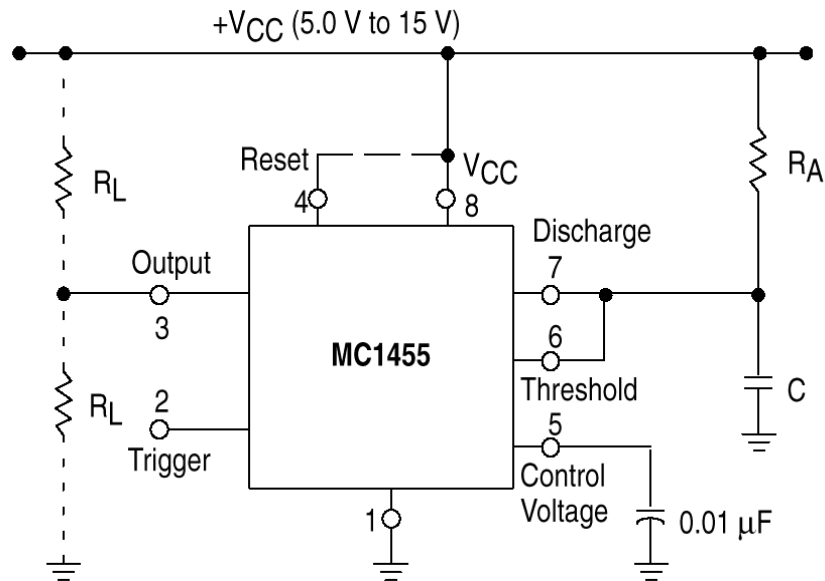


Fig. 204. Monostable MV using 555 timer (Fig. 200 repeated).

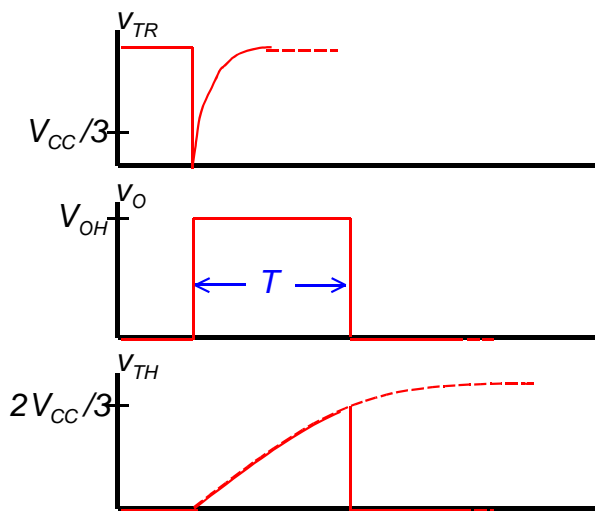


Fig. 205. Monostable waveforms.

Other comments . . .

Output pulse may be terminated early if reset pin brought low.

Trigger pulse must remain below $V_{CC}/3$ for 50-100 ns.

Control voltage input (V_{CV}) can be used to alter timing, in which case:

$$p = \frac{V_{CC} - V_{CV}}{V_{CC}} \quad (233)$$

Leakage, Bias, and Discharge Currents:

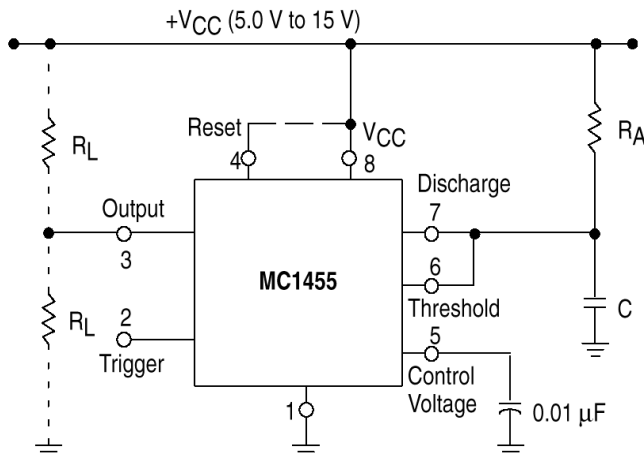


Fig. 206. Monostable MV using 555 timer (Fig. 200 repeated).

The input bias currents are:

For the threshold comparator:
approximately $0.25 \mu\text{A}$

For the trigger comparator:
approximately $1.5 \mu\text{A}$

The capacitor is not ideal, but has leakage current. The amount of leakage current depends on the type of C

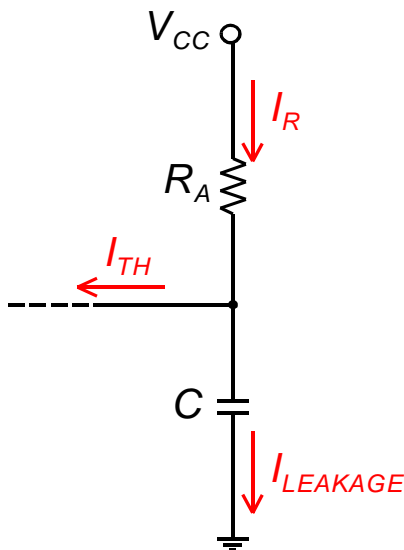


Fig. 207. Bias and leakage currents.

For accurate timing, we want:

$$I_R \gg I_{LEAKAGE} + I_{TH} \quad (234)$$

Note that I_R is smallest for $V_{TH} = 2V_{CC}/3$.

We can estimate the largest practical R_A :

Assume $V_{CC} = 15 \text{ V}$, $I_{LEAKAGE} = 0.25 \mu\text{A}$

For $I_R \gg I_{LEAKAGE} + I_{TH}$, we let:

$$I_R \geq 5 \mu\text{A} \text{ at } V_{TH} = 10 \text{ V}$$

Then

$$R_A \leq \frac{15 \text{ V} - 10 \text{ V}}{5 \mu\text{A}} = 1 \text{ M}\Omega \quad (235)$$

We must also keep $R_A \geq 5 \text{ k}\Omega$ (or so), to limit $Q_{discharge}$ current.

Triggering in Monostable Mode:

1. Negative Trigger Pulse - If the trigger pulse is shorter than the output pulse, a direct connection is OK.

But if the trigger pulse is longer than the output pulse, a direct connection would result in simultaneous trigger and threshold commands. The state of v_o would be unknown.

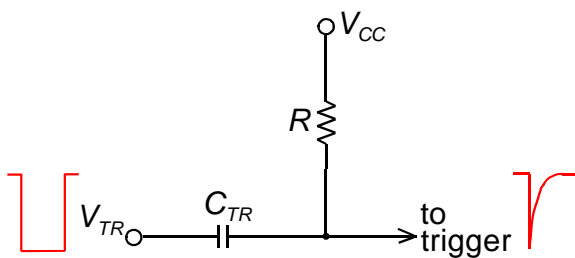


Fig. 208. RC-coupled trigger pulse.

RC-coupling allows V_{TR} to be well above $V_{CV}/2$ by end of timing cycle.

Typically, τ should be > 10 ns.

2. Positive Trigger Pulse - In this case we can apply the pulse to both the trigger input and the reset input.

On leading edge of the trigger pulse, reset input goes high *before* trigger input does, allowing an active timer to be triggered.

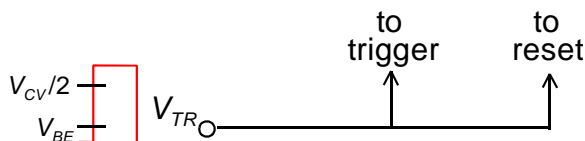


Fig. 209. Positive trigger pulse.

However, the trigger pulse must be longer than output pulse.

Otherwise an additional inverting circuit must be used to provide a negative trigger.

Astable Multivibrator

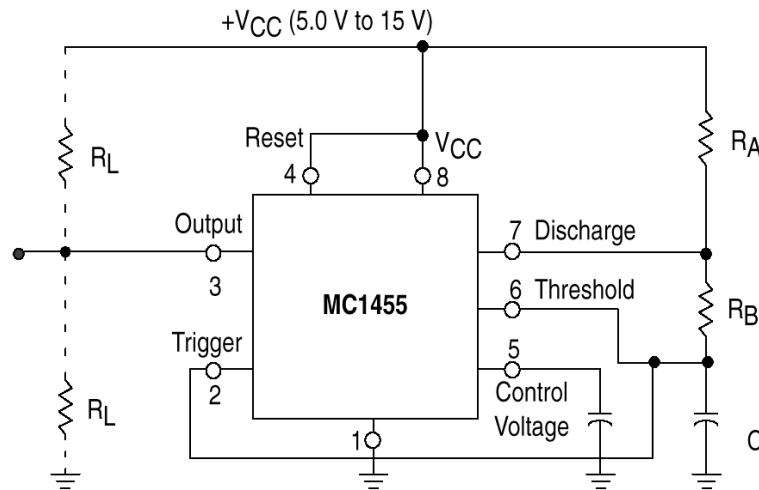


Fig. 210. Astable MV using 555 timer.

The astable multivibrator generates a free-running rectangular waveform, i.e., it is an oscillator.

Operation:

We'll assume steady-state, with:

$$v_O = V_{OH}, \quad Q_{\text{discharge}} \text{ off}$$

The capacitor charges toward V_{CC} through R_A and R_B until $v_C = 2V_{CC}/3$

Thus:

$$t_H = \tau_1 \ln \frac{1}{p_H} \quad (236)$$

where:

$$\tau_1 = (R_A + R_B)C \quad \text{and} \quad p_H = \frac{V_{CC} - \frac{2}{3}V_{CC}}{V_{CC} - \frac{1}{3}V_{CC}} = \frac{1}{2} \quad (237)$$

Thus:

$$t_H = (R_A + R_B)C \ln 2 \quad (238)$$

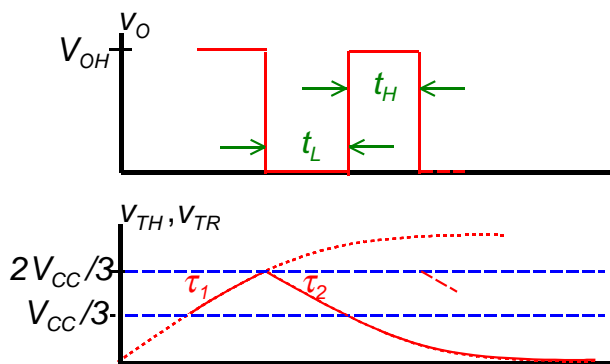


Fig. 211. Astable waveforms.

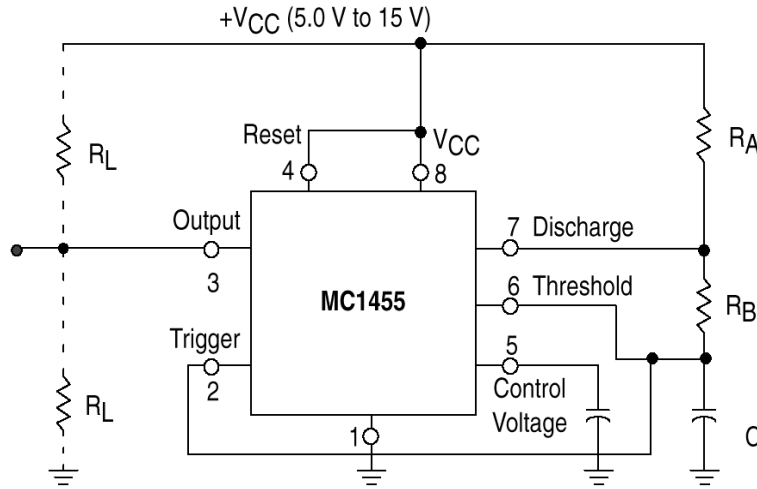


Fig. 212. Astable MV using 555 timer (Fig. 210 repeated).

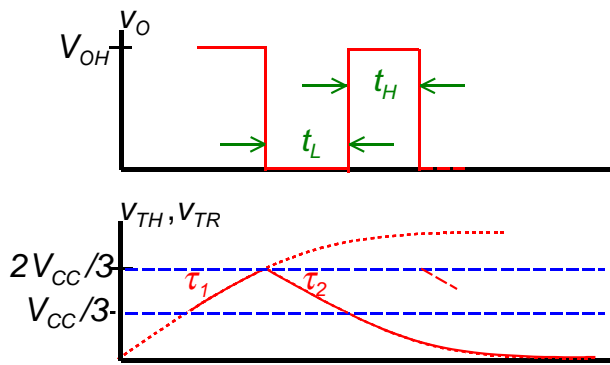


Fig. 213. Astable waveforms (Fig. 211 repeated).

Now v_C has reached $2V_{CC}/3$, and the timer changes state. The flip-flop resets, with:

$$v_O = V_{OL} \approx 0, \quad Q_{\text{discharge}} \text{ on}$$

Now, C charges only thru R_B toward zero: Thus:

$$t_L = \tau_2 \ln \frac{1}{\rho_L} \quad (239)$$

where

$$\tau_2 = R_B C \quad \text{and} \quad \rho_L = \frac{\frac{1}{3}V_{CC} - 0}{\frac{2}{3}V_{CC} - 0} = \frac{1}{2} \quad (240)$$

Thus:

$$t_L = R_B C \ln 2 \quad (241)$$

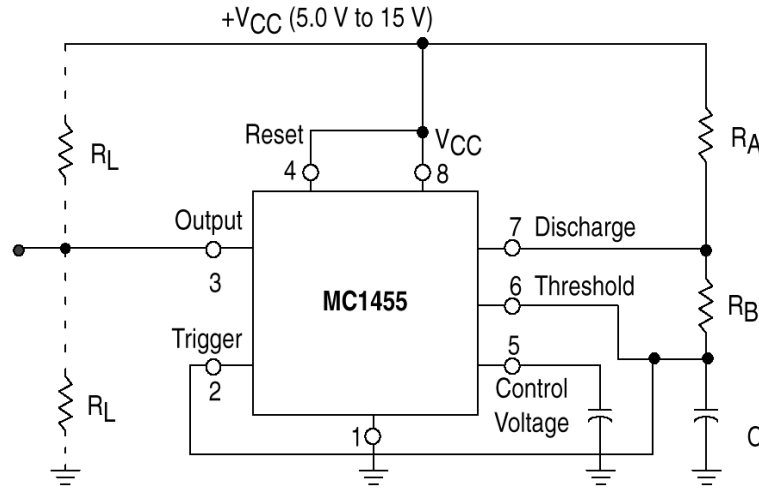


Fig. 214. Astable MV using 555 timer (Fig. 210 repeated).

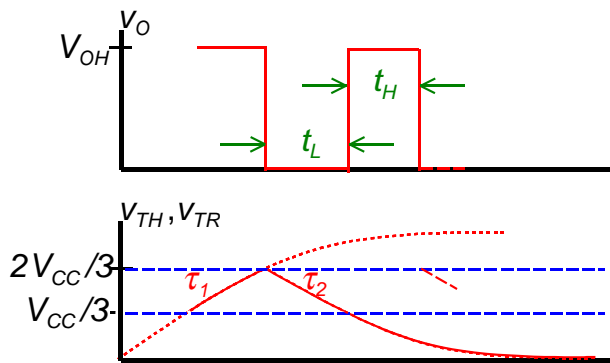


Fig. 215. Astable waveforms (Fig. 211 repeated).

Finally, we combine eq. (238) and eq. (241) to calculate frequency and duty ratio:

$$f = \frac{1}{T} = \frac{1}{t_H + t_L} = \frac{1}{(R_A + 2R_B)C \ln 2} \quad (242)$$

And

$$D = \frac{t_H}{T} = \frac{R_A + R_B}{R_A + 2R_B} \quad (243)$$

Notice that D must be between 0.5 and 1. It approaches 0.5 for $R_A \ll R_B$, and 1 for $R_A \gg R_B$. We can achieve duty ratios less than 0.5 only by varying the control voltage.

Varying the Control Voltage:

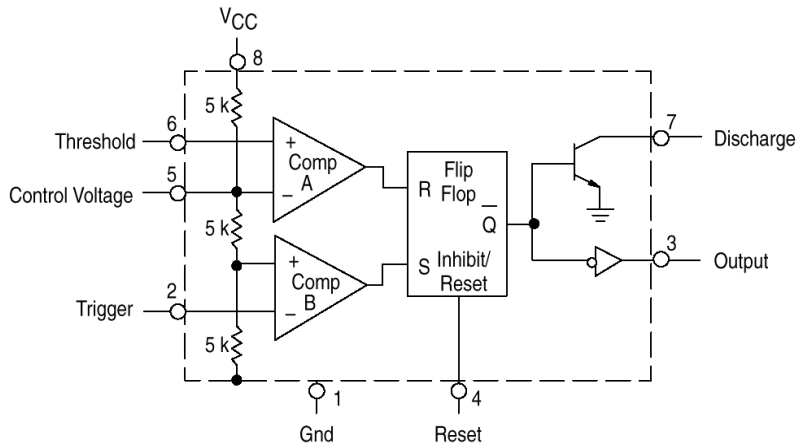


Fig. 216. Function diagram of 555 timer (Fig. 198 repeated).

Recall that the CV input is the reference to the threshold comparator.

It is also connected to upper junction of the voltage divider.

Note also that the reference to the trigger comparator is always half of the threshold comparator reference.

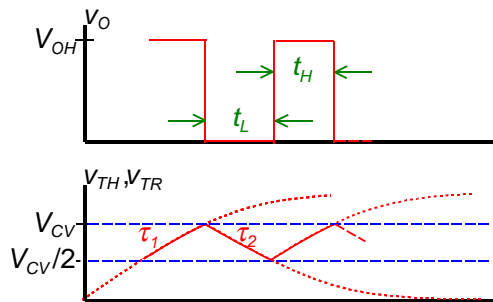


Fig. 217. Astable waveforms with change in notation for switching levels.

Thus, t_L won't change with changes in V_{CV} ! But:

If V_{CV} increases, t_H increases,

If V_{CV} decreases, t_H decreases

So we can change f and D directly, by varying V_{CV} !!!

The two most common techniques used to vary the control voltage are shown on the following pages.

There are 2 basic ways to change the control voltage . . .

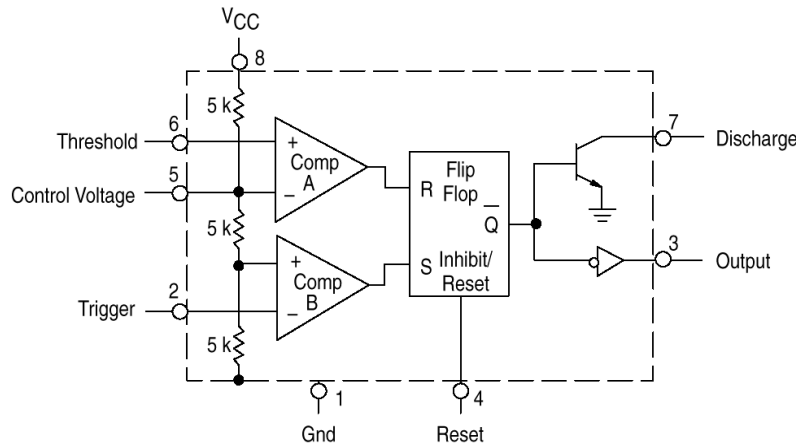


Fig. 218. Function diagram of 555 timer (Fig. 198 repeated).

1. The simple (but less accurate) way:

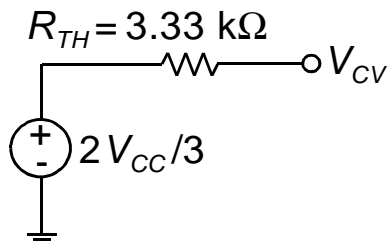


Fig. 219. Thevenin Eq. of internal divider.

Note that the internal voltage divider can be represented by its Thevenin Equivalent.

We can add a pull-up resistor from V_{CV} to V_{CC} to increase the control voltage, or

we can add a pull-down resistor from V_{CV} to ground to decrease the control voltage.

Problem: the internal resistors are not known accurately.

Solution: attach a *voltage source* to the control voltage pin.

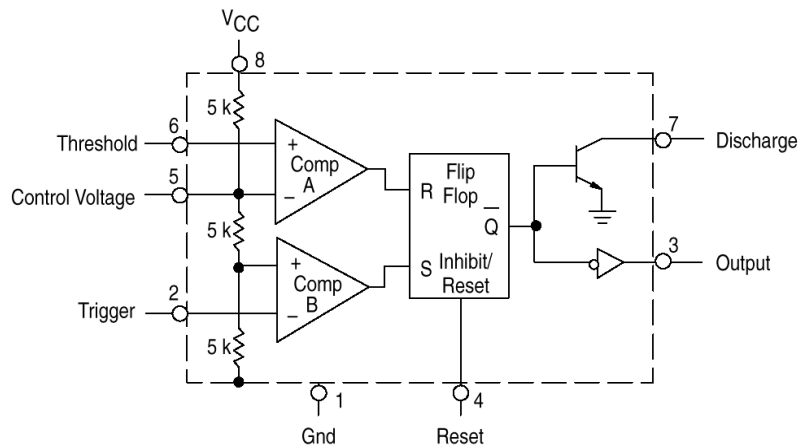


Fig. 220. Function diagram of 555 timer (Fig. 198 repeated).

2. Controlling V_{CV} with a voltage source:

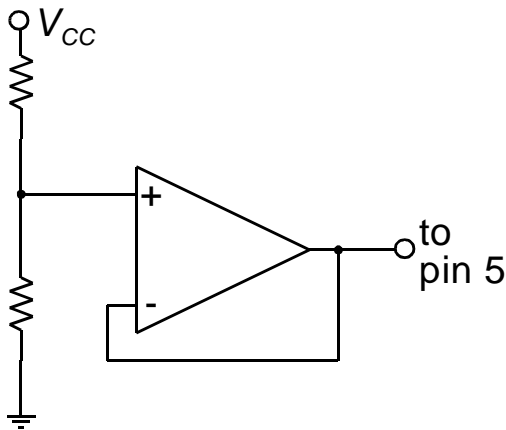


Fig. 221. Setting V_{CV} with a voltage source.

The op amp voltage follower serves as a voltage source.

The resistive divider keeps V_{CV} a fixed fraction of V_{CC} so that circuit operation remains independent of V_{CC} .

We might even choose resistors with equal temperature coefficients.

Energy Storage Elements

Here we review some interesting behaviors in capacitive and inductive circuits . . .

Capacitor in Series with Arbitrary Impedance

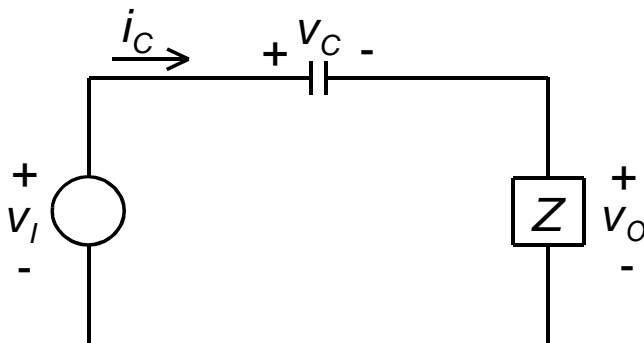


Fig. 222. Capacitor in series with arbitrary Z .

Recall the basic current-voltage relationship:

$$i_C = C \frac{dv_C}{dt} \quad (244)$$

We make the following interpretations from the equation:

- Current i_C must be *finite* i.e., there are no current impulses (presuming v_I contains no impulses). Thus:

The voltage v_C is *continuous*, i.e., there are no step changes, i.e., $\Delta v_C = 0$.

Any step change in v_I must equal the step change in v_O , i.e., $\Delta v_I = \Delta v_O$.

- If i_C is constant, the capacitor voltage is a ramp function.

Inductor in Parallel with Arbitrary Impedance

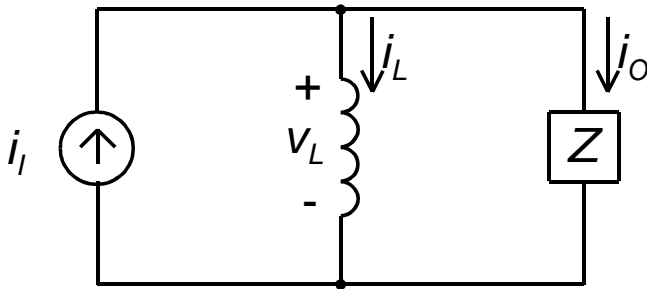


Fig. 223. Inductor in parallel with arbitrary Z .

Recall the basic current-voltage relationship:

$$v_L = L \frac{di_L}{dt} \quad (245)$$

We make the following interpretations from the equation:

- Voltage v_L must be *finite*, i.e., there are no voltage impulses (presuming i_L contains no impulses). Thus:

The current i_L is continuous, i.e., there are no step changes, i.e., $\Delta i_L = 0$.

Any step change in i_i must equal the step change in i_o , i.e., $\Delta i_i = \Delta i_o$.

- If v_L is constant, the inductor current is a ramp function.
- This is merely the dual of the previous example.

Capacitive Voltage Divider

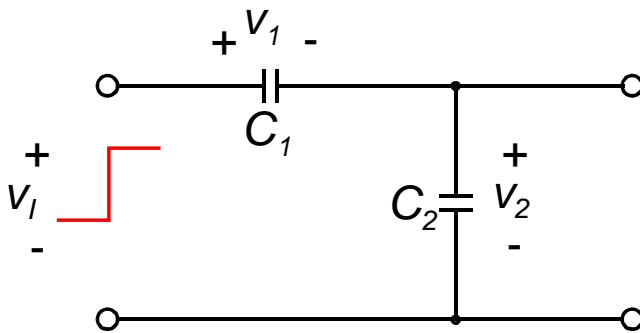


Fig. 224. Capacitive voltage divider.

Recall the basic current-voltage relationship:

$$v_C = \frac{1}{C} \int i_C dt \quad (246)$$

We make the following interpretations from the equation, assuming an input voltage step, as shown above:

- The input voltage step divides in inverse proportion to C .
- The current is an impulse, and

$$\Delta v_1 = \Delta v_I \frac{C_2}{C_1 + C_2} \quad \text{and} \quad \Delta v_2 = \Delta v_I \frac{C_1}{C_1 + C_2} \quad (247)$$

The dual of this circuit is the inductive current divider, however, it is not discussed here

Miscellany

- Any elements in parallel with a voltage source do not affect the remaining circuit.
- Any elements in series with a current source do not affect the remaining circuit.

RC Attenuators

RC attenuators are important circuits for use with general waveforms, especially pulse and rectangular waveforms. Of these, the compensated attenuator is most important and the easiest to study, so it is where we begin.

The Compensated Attenuator

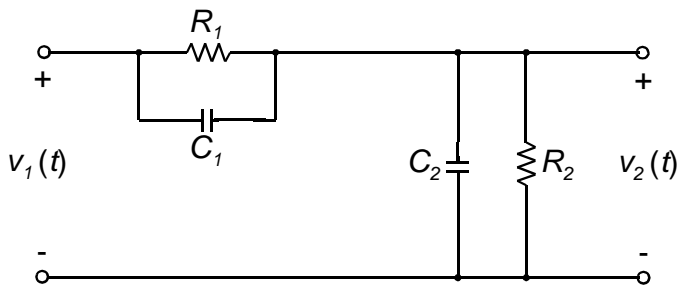


Fig. 225. The compensated attenuator.

We begin by defining:

$$\tau_1 = R_1 C_1 \quad (248)$$

and

$$\tau_2 = R_2 C_2 \quad (249)$$

For a compensated attenuator we require that $\tau_1 = \tau_2$.

To help with the mathematical development, let's recall that for any parallel RC combination we have:

$$Z(s) = \frac{R \left(\frac{1}{sC} \right)}{R + \frac{1}{sC}} = \frac{\frac{1}{C}}{s + \frac{1}{RC}} = \frac{1}{C \left(s + \frac{1}{\tau} \right)} \quad (250)$$

Thus, we may write:

$$Z_1(s) = R_1 \parallel C_1 = \frac{1}{C_1 \left(s + \frac{1}{\tau_1} \right)}, \quad Z_2(s) = R_2 \parallel C_2 = \frac{1}{C_2 \left(s + \frac{1}{\tau_2} \right)} \quad (251)$$

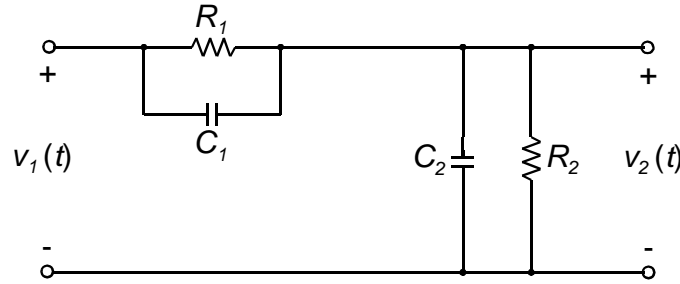


Fig. 226. The compensated attenuator (Fig. 225 repeated).

The transfer function is:

$$H(s) = \frac{V_2(s)}{V_1(s)} = \frac{Z_2(s)}{Z_1(s) + Z_2(s)} = \frac{\frac{1}{C_2 \left(s + \frac{1}{\tau_2} \right)}}{\frac{1}{C_1 \left(s + \frac{1}{\tau_1} \right)} + \frac{1}{C_2 \left(s + \frac{1}{\tau_2} \right)}} \quad (252)$$

Because $\tau_1 = \tau_2$, the $(s + 1/\tau)$ terms in the above equation will cancel, leaving:

$$H(s) = \frac{\frac{1}{C_2}}{\frac{1}{C_1} + \frac{1}{C_2}} = \frac{C_1}{C_1 + C_2} = \frac{\frac{\tau}{R_1}}{\frac{\tau}{R_1} + \frac{\tau}{R_2}} = \frac{R_2}{R_1 + R_2} \quad (253)$$

Note that $H(s)$ is independent of s , i.e., constant for all frequency, with the ratio of the capacitive voltage divider or the resistive voltage divider.

This means $v_2(t)$ will always be an attenuated replica of $v_1(t)$, regardless of the type of waveform of $v_1(t)$!!!

The Generalized RC Attenuator

With a little more effort, we can generalize the previous result.

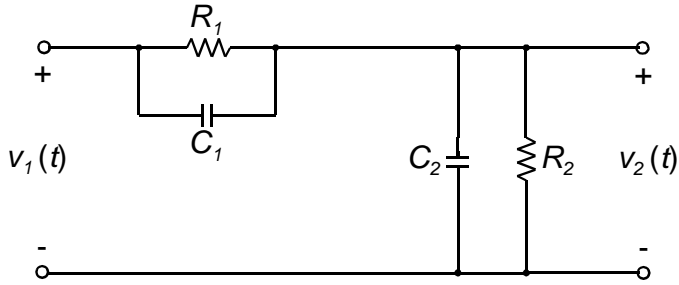


Fig. 227. A generalized RC attenuator.

Again we let

$$\tau_1 = R_1 C_1 \quad (254)$$

and

$$\tau_2 = R_2 C_2 \quad (255)$$

and, for convenience, we add the additional expression:

$$\tau = R_{eq} C_{eq} = (R_1 \parallel R_2)(C_1 + C_2) \quad (256)$$

Also, as before, we have

$$Z_1(s) = R_1 \parallel C_1 = \frac{1}{C_1 \left(s + \frac{1}{\tau_1} \right)}, \quad Z_2(s) = R_2 \parallel C_2 = \frac{1}{C_2 \left(s + \frac{1}{\tau_2} \right)} \quad (257)$$

Now, the transfer function is:

$$H(s) = \frac{\frac{1}{C_2 \left(s + \frac{1}{\tau_2} \right)}}{\frac{1}{C_1 \left(s + \frac{1}{\tau_1} \right)} + \frac{1}{C_2 \left(s + \frac{1}{\tau_2} \right)}} = \frac{C_1 \left(s + \frac{1}{\tau_1} \right)}{C_1 \left(s + \frac{1}{\tau_1} \right) + C_2 \left(s + \frac{1}{\tau_2} \right)} \quad (258)$$

Working with just the denominator of $H(s)$:

$$\begin{aligned}
 C_1 \left(s + \frac{1}{\tau_1} \right) + C_2 \left(s + \frac{1}{\tau_2} \right) &= C_1 s + C_2 s + \frac{C_1}{\tau_1} + \frac{C_2}{\tau_2} \\
 &= (C_1 + C_2) s + \frac{1}{R_1} + \frac{1}{R_2} = (C_1 + C_2) s + \frac{1}{R_1 \parallel R_2} \\
 (C_1 + C_2) s + \frac{C_{eq}}{\tau} &= (C_1 + C_2) s + \frac{C_1 + C_2}{\tau} \\
 &= (C_1 + C_2) \left(s + \frac{1}{\tau} \right)
 \end{aligned} \tag{259}$$

Thus, the transfer function becomes:

$$H(s) = \frac{C_1 \left(s + \frac{1}{\tau_1} \right)}{(C_1 + C_2) \left(s + \frac{1}{\tau} \right)} \tag{260}$$

Now, at dc, $s = 0$, and:

$$H(0) = \frac{\frac{C_1}{\tau_1}}{\frac{(C_1 + C_2)}{\tau}} = \frac{\frac{1}{R_1}}{\frac{1}{R_1 \parallel R_2}} = \frac{\frac{1}{R_1}}{\frac{R_1 + R_2}{R_1 R_2}} = \frac{R_2}{R_1 + R_2} = K_R \tag{261}$$

Thus, for dc, the transfer function is merely a resistive voltage divider, as expected.

Now, as s becomes infinite:

$$\lim_{s \rightarrow \infty} H(s) = \frac{C_1 s}{(C_1 + C_2)s} = \frac{C_1}{C_1 + C_2} = K_C \quad (262)$$

Thus for infinite frequency (like the edge of a step function), the transfer function is merely a capacitive voltage divider, as expected.

The significance of K_R and K_C becomes more apparent when we look at the poles and zeros of $H(s)$.

Poles and Zeros:

Recall $H(s)$:

$$H(s) = \frac{C_1 \left(s + \frac{1}{\tau_1} \right)}{(C_1 + C_2) \left(s + \frac{1}{\tau} \right)} \quad (263)$$

This has a zero at $s_Z = -1/\tau_1$ and a pole at $s_P = -1/\tau$. Now we look at the ratio of s_P to s_Z :

$$\begin{aligned} \frac{s_P}{s_Z} &= \frac{-\frac{1}{\tau}}{-\frac{1}{\tau_1}} = \frac{\frac{1}{(R_1 \parallel R_2)(C_1 + C_2)}}{\frac{1}{R_1 C_1}} = \frac{1}{\frac{R_1 R_2}{R_1 + R_2} (C_1 + C_2)} \cdot \frac{R_1 C_1}{1} \\ &= \frac{C_1}{\frac{R_2}{R_1 + R_2} (C_1 + C_2)} = \frac{K_C}{K_R} \end{aligned} \quad (264)$$

Eq. (264) shows that:

- For $K_C < K_R$ (called undercompensated), $s_P < s_Z$
- For $K_C > K_R$ (called overcompensated), $s_P > s_Z$

We can illustrate this with Bode magnitude plots:

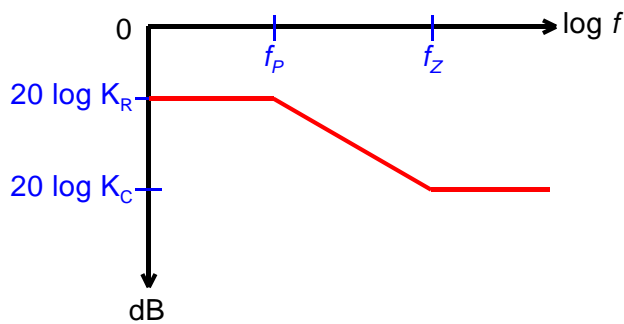


Fig. 228. Undercompensated RC attenuator, $K_C < K_R$, $s_P < s_Z$.

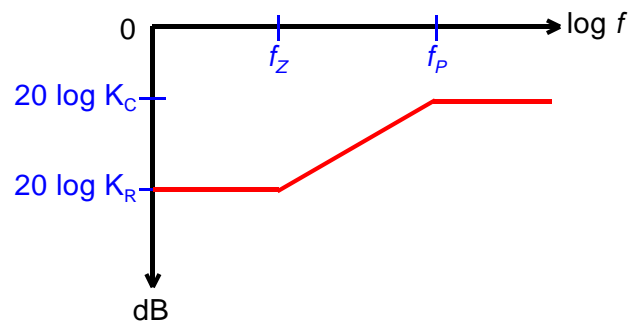


Fig. 229. Overcompensated RC attenuator, $K_C > K_R$, $s_P > s_Z$.

Note that:

- The undercompensated attenuator has a lowpass effect
- The overcompensated attenuator has a highpass effect
- For a compensated attenuator, $K_C = K_R$, $s_P = s_Z$, and the Bode magnitude plot will merely be a horizontal line at $20 \log K_C = 20 \log K_R$.

Thus it will not alter the frequency components of any waveform, which is the same as saying $v_2(t)$ will always be an attenuated replica of $v_1(t)$, regardless of the type of waveform of $v_1(t)$!!!

We can see the lowpass and highpass effects by looking at the general response of an RC attenuator to a rectangular wave input.

Undercompensated Attenuator Rectangular-Wave Response:

$K_C < K_R$. Thus the step sizes of the output waveform are smaller than $(K_R V_{1H} - K_R V_{1L}) = K_R V_{1PP}$:

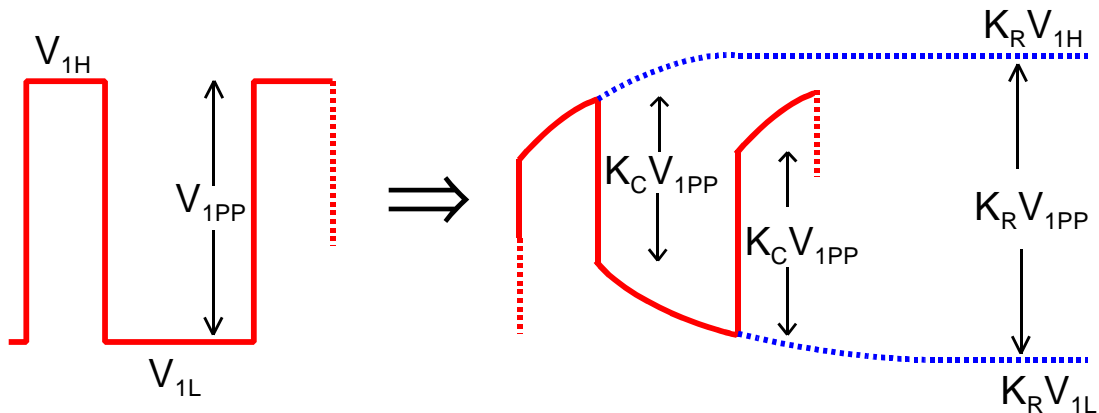


Fig. 230. Undercompensated attenuator rectangular-wave response.

Overcompensated Attenuator Rectangular-Wave Response:

$K_C > K_R$. Thus the step sizes of the output waveform are larger than $(K_R V_{1H} - K_R V_{1L}) = K_R V_{1PP}$:

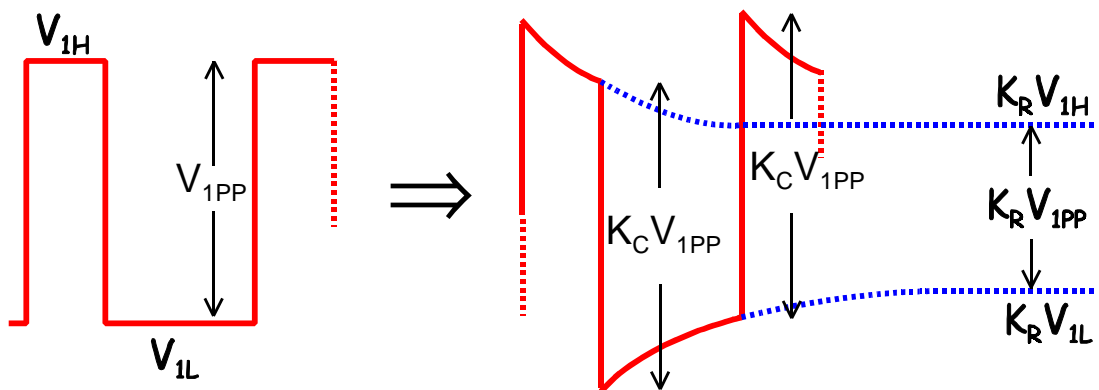


Fig. 231. Overcompensated attenuator rectangular-wave response.

Practical RC Attenuators

A practical RC attenuator is not driven by an ideal voltage source but, rather, by a source which includes its internal resistance:

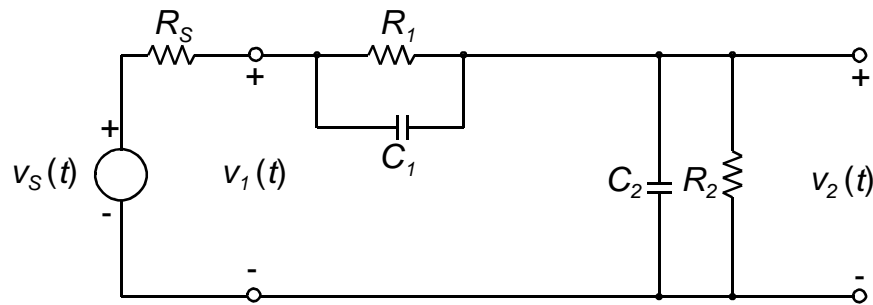


Fig. 232. Practical RC attenuator circuit.

In general this is not a single-pole circuit. But we can show that it becomes a single-pole circuit if compensated, by re-drawing the above figure:

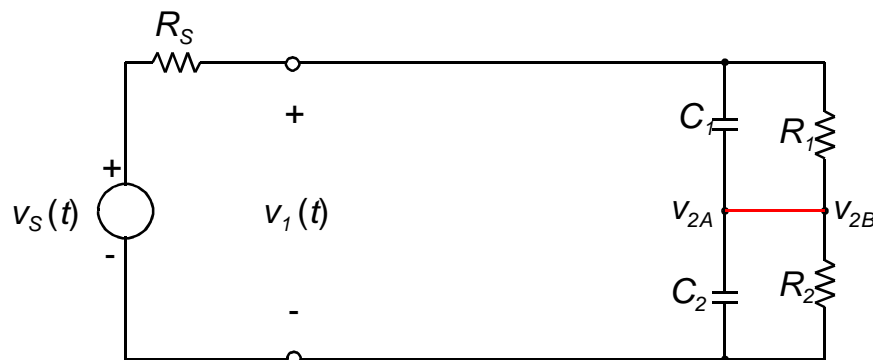


Fig. 233. Practical RC attenuator circuit re-drawn.

If the attenuator is precisely compensated we will have $\tau_1 = \tau_2$ (i.e., $R_1 C_1 = R_2 C_2$). Then we will also have $K_C = K_R$ and voltage v_{2A} will equal voltage v_{2B} even with the connection between them removed.

With the connection removed, we can see that there is a single equivalent capacitance. Therefore we have a single-pole circuit!!!

An Oscilloscope Probe Example

An *RC* attenuator has many uses, the most common of which is the *oscilloscope / oscilloscope probe* combination.

Lets first look at a step voltage source connected directly to an oscilloscope input:

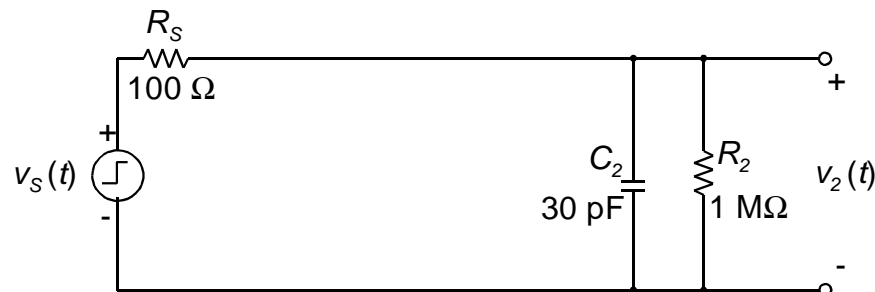


Fig. 234. Step voltage source connected to oscilloscope. R_2 and C_2 represent the scope input impedance. Typical values are shown.

The time constant of this circuit is:

$$\tau = 30\text{pF}(100\Omega \parallel 1\text{M}\Omega) \approx 30\text{pF}(100\Omega) = 3\text{ns} \quad (265)$$

and the resulting rise time of v_2 is:

$$t_r = \tau \ln \frac{1}{p} = \tau \ln 9 = 6.59\text{ns} \quad (266)$$

Thus, the step input will appear on the oscilloscope as an exponential, single-pole response.

Now we measure the same step input, v_S , with a 10X oscilloscope probe. This is nothing more than a 10:1 compensated attenuator which produces $K_C = K_R = 10$:

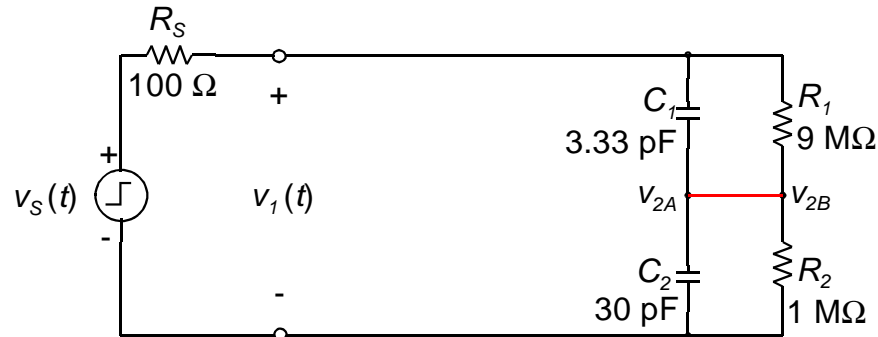


Fig. 235. 10X oscilloscope probe inserted between voltage source and oscilloscope.

This is a perfectly compensated attenuator, so we can remove the short-circuit (shown in red). This leaves a single-pole circuit with:

$$C_{eq} = \frac{(3.33\text{pF})(30\text{pF})}{3.33\text{pF} + 30\text{pF}} = 3\text{pF} \quad (267)$$

The time constant of this circuit is:

$$\tau = 3\text{pF}(100\Omega \parallel 10\text{M}\Omega) \approx 3\text{pF}(100\Omega) = 300\text{ps} \quad (268)$$

Because v_2 is an attenuated replica of v_1 , both voltages will have the same rise time:

$$t_r = \tau \ln 9 = 659\text{ps} \quad (269)$$

The oscilloscope response is ten times faster using the 10X probe!!! The price we pay for this improvement is a smaller amplitude signal at v_2 .

Diode Static Characteristics

Recall that the diode i - v characteristic is described by the Shockley equation:

$$i_D = I_S \left[\exp\left(\frac{V_D}{nV_T}\right) - 1 \right] \quad (270)$$

where I_S is the reverse saturation current, and

$$V_T = \frac{kT}{q} \approx 25\text{mV} \quad \text{at} \quad T = 300\text{K} \quad (271)$$

Measuring Reverse Saturation Current

Attempts to measure this directly result in values much larger than I_S , due to surface leakage current, but I_S can be obtained from forward bias measurements in the following manner.

Beginning with the forward bias approximation:

$$i_D \approx I_S \exp\left(\frac{V_D}{nV_T}\right) \quad (272)$$

We then find the natural logarithm of both sides:

$$\ln i_D = \ln I_S + \frac{V_D}{nV_T} \quad (273)$$

And change to common (i.e., base 10) logarithms:

$$2.3 \log i_D = 2.3 \log I_S + \frac{V_D}{nV_T} \quad (274)$$

$$\log i_D = \left(\frac{1}{2.3nV_T} \right) V_D + \log I_S$$

Comparing the final form of eq. (274):

$$\log i_D = \left(\frac{1}{2.3nV_T} \right) v_D + \log I_S \quad (275)$$

to the standard notation describing the equation of a straight line:

$$y = mx + b \quad (276)$$

we see that the diode forward i - v characteristic should be a straight line when i_D is plotted on the log axis of a *semi-log* graph, and the y -axis intercept is the common logarithm of I_S !!!

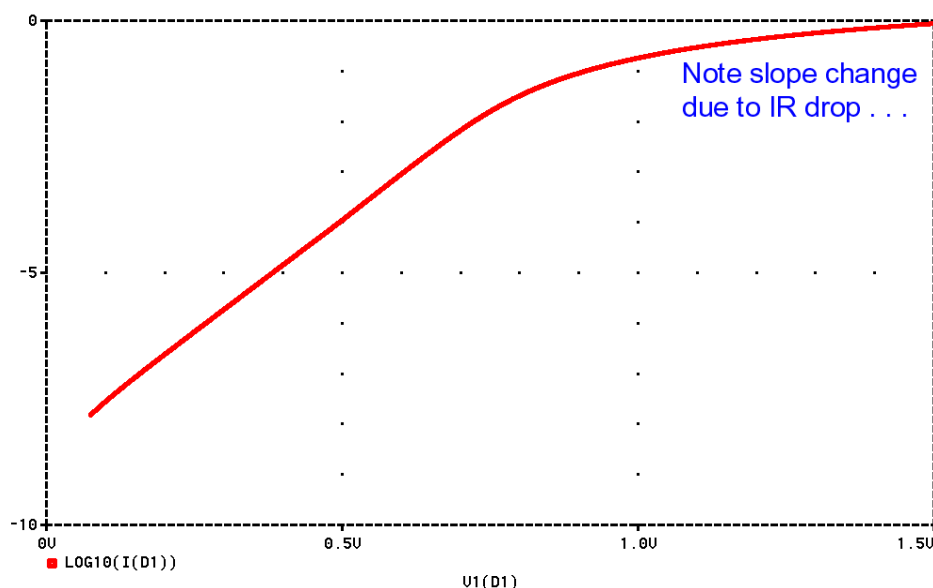


Fig. 236. PSpice-simulated “semi-log” i - v characteristic of 1N4148 diode.

With laboratory data, the straight line we use should be a least-squared-error fit at low and moderate currents, to avoid the influence of the semiconductor IR drop at higher currents.

Typical I_S values are within two or three decades of 10 fA.

Diode Cut-in Voltage

From observation, for small-signal diodes, a nominal diode voltage of 0.75 V results in a nominal diode current of 10 mA. Assuming $n = 1$ we could write:

$$i_{NOMINAL} = I_S \exp\left(\frac{V_{NOMINAL}}{V_T}\right) \quad (277)$$

For diodes to be used as a switch, let us define the off state to be when i_D is less than 1% of the nominal value. We define the corresponding voltage as the cut-in voltage:

$$0.01i_{NOMINAL} = I_S \exp\left(\frac{V_{CUT-IN}}{V_T}\right) \quad (278)$$

Dividing eq. (277) by eq. (278) and solving for v_{CUT-IN} :

$$100 = \exp\left(\frac{V_{NOMINAL} - V_{CUT-IN}}{V_T}\right) \quad (279)$$

$$V_{NOMINAL} - V_{CUT-IN} = V_T \ln 100 = 115 \text{ mV}$$

Thus $v_{CUT-IN} \approx 0.75 \text{ V} - 0.115 \text{ V} = 0.635 \text{ V}$. For the base-emitter diode of BJTs, we round this value to arrive at these typical assumptions:

$$v_{BE} < 0.65 \text{ V} \Rightarrow \text{cutoff}$$

$$v_{BE} = 0.70 \text{ V} \Rightarrow \text{active}$$

$$v_{BE} > 0.75 \text{ V} \Rightarrow \text{saturation}$$

Temperature Dependence

For a constant diode current:

$$\frac{\partial v_D}{\partial T} = -2 \frac{\text{mV}}{\text{K}} \quad (280)$$

Depletion Capacitance

With the symbol C_j (presumably for *junction capacitance*, by which this is also known), this capacitance arises from the bound charges that exist in the depletion region under reverse bias (and low forward bias). It is given by:

$$C_j = \frac{C_{j0}}{\left(1 - \frac{V_{DQ}}{\Phi_0}\right)^m} \quad (281)$$

where C_{j0} is the *zero-bias depletion capacitance* ($\approx 4 \text{ pF}$)

V_{DQ} is the diode quiescent voltage

Φ_0 is the *built-in barrier potential* ($\approx 1 \text{ V}$)

and m is the *grading coefficient* (≈ 0.5)

(Values in parentheses are typical for the 1N4148 diode)

In addition to the term *junction capacitance*, depletion capacitance is also called *transition capacitance*, and *barrier capacitance*.

A plot of eq. (281), normalized to C_{j0} for the values given above, is shown on the following page.

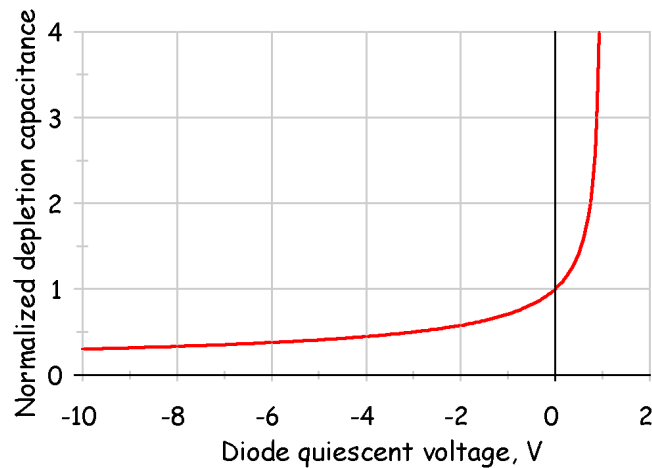


Fig. 237. Typical normalized depletion capacitance vs. diode voltage.

Diffusion Capacitance

This arises from the charges which diffuse across the junction under forward bias. It is very important in the base-emitter diode of BJT amplifiers (C_π), but of little importance in diodes used for switching. It will not be considered here.

Zener Diodes

Recall that there are two different mechanisms for breakdown:

- Avalanche breakdown ($V_Z > 6$ V), due to kinetic energy of carriers, produces curves with sharper knees.
- Zener breakdown ($V_Z < 6$ V), due to high E field.
- The temperature coefficient of zener diodes is approximately $(V_Z - 5)$ mV/K.

IC Diodes

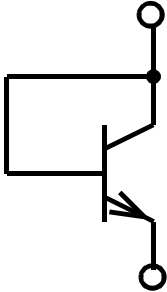


Fig. 238.
IC diode.

It is not economical to use a different masking for diodes than that already used for transistors, so transistors are simply wired to function as diodes.

Of all possible connections, the connection shown at left has:

- lowest forward drop
- fastest switching,
- lowest C_j
- BV_{EB} from 6 V to 9 V

BJT Static Characteristics

Let's review the basics of BJTs:

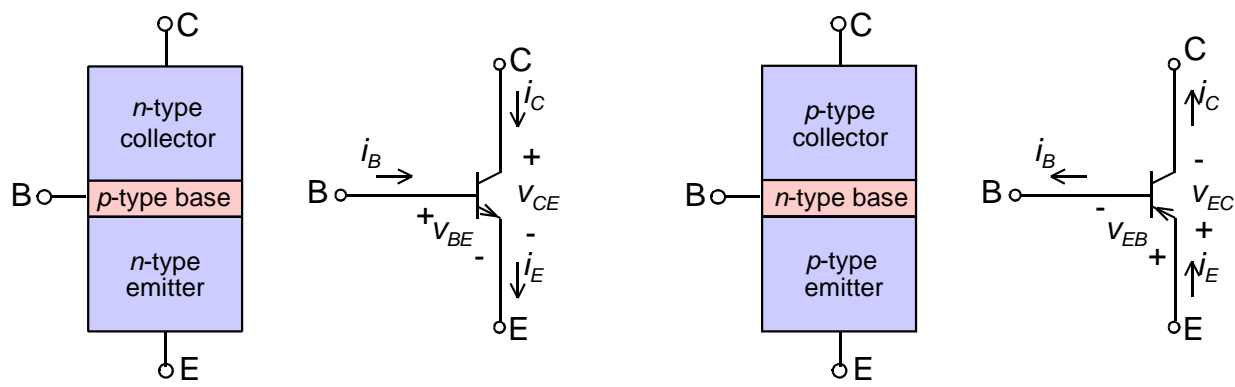


Fig. 239. *Npn* and *pnp* (left and right, respectively) bipolar junction transistors.

Operating Region	EBJ	CBJ	Feature
cutoff	rev.	rev.	$i_C = i_E = i_B = 0$
active	fwd.	rev.	$i_C = h_{FE} i_B$
saturation	fwd.	fwd.	$i_C < h_{FE} i_B$
inverse	rev.	fwd.	$i_C < 0$, very small

Notes:

- At the active-saturation boundary, $v_{CB} = 0$ and $i_C = h_{FE} i_B$.
- $$h_{FE} = \frac{i_C}{i_B} \quad \text{and} \quad h_{fe} = \frac{\partial i_C}{\partial i_B} = \frac{i_c}{i_b} \tag{282}$$
- $h_{FE} = h_{fe}$ in the normal temperature range for silicon devices.
- h_{FE} variation of 10:1 possible . . . 3:1 typical.

Output Characteristics

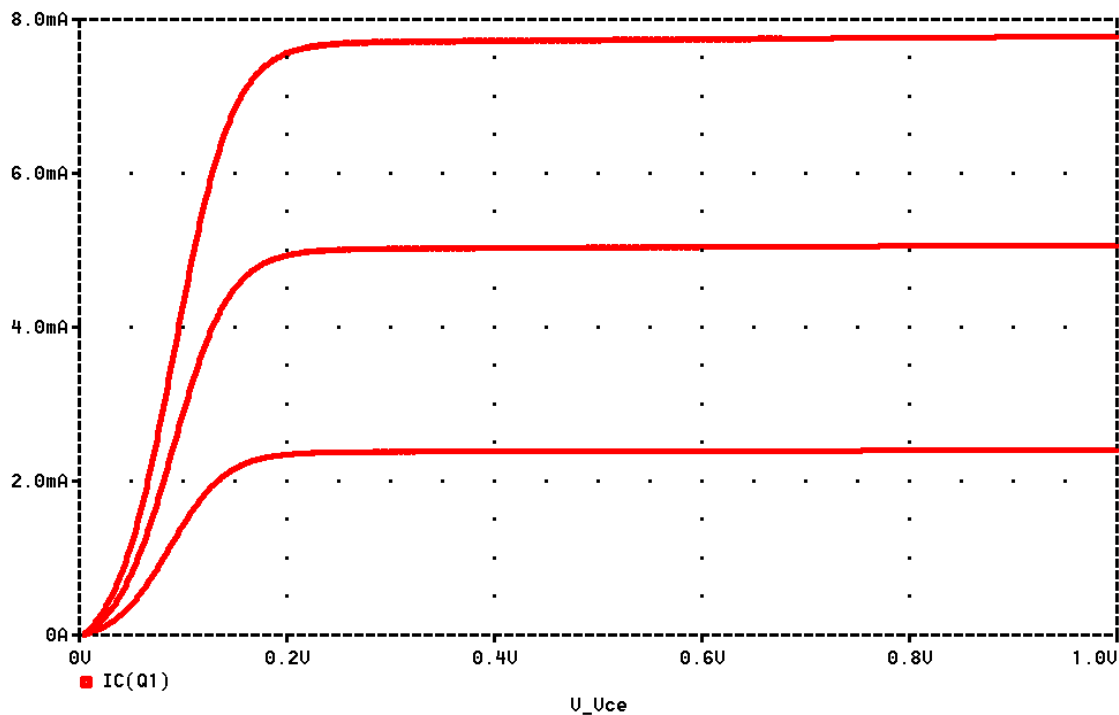


Fig. 240. BJT output characteristics in the saturation and near-saturation regions.

- With i_B fixed, i_C is a function of v_{CE} , and with v_{CE} fixed, i_C is a function of i_B .
- The curves do not go through the origin, rather, $i_C = 0$ for $v_{CE} = \text{few mV}$.
- There is no mathematical model for the saturation region that is simple and accurate.

For high accuracy we should use PSpice, or an equivalent.

For easy, but more approximate, analysis we can use a simple piecewise-linear model.

BJT Saturation-Region Model

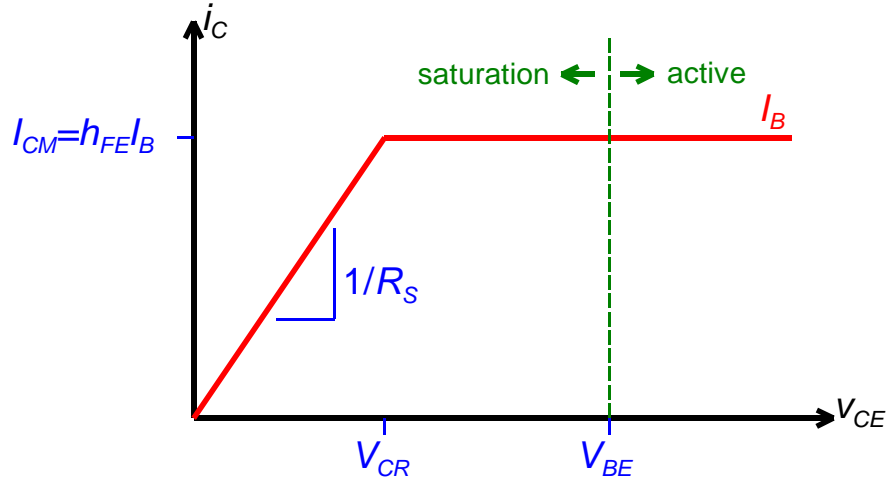


Fig. 241. Piecewise-linear approximation to BJT output characteristics

For the saturation-region piecewise-linear model, we define the corner voltage, V_{CR} , which is typically 0.2 V to 0.4 V.

Our default value for the corner voltage is $V_{CR} = 0.3\text{V}$.

We also define the saturation resistance:

$$R_S = \frac{V_{CR}}{h_{FE} I_B} \quad (283)$$

thus

$$\begin{aligned} i_C &= \frac{V_{CE}}{R_S} = \frac{h_{FE} I_B}{V_{CR}} V_{CE}, \quad 0 \leq v_{CE} \leq V_{CR} \\ &= h_{FE} I_B, \quad V_{CR} \leq v_{CE} \leq BV_{CEO} \end{aligned} \quad (284)$$

Note that the Early effect is ignored. It is important in analog circuits, but not in switching circuits.

BJT Example

We let $V_{CR} = 0.3 \text{ V}$ and $V_{BE} = 0.7 \text{ V}$ for the BJT in the circuit below, and calculate the collector-emitter voltage for various base currents.

Note that the load line equation for this circuit is:

$$10 \text{ V} - i_C (1\text{k}\Omega) = v_{CE} \quad (285)$$

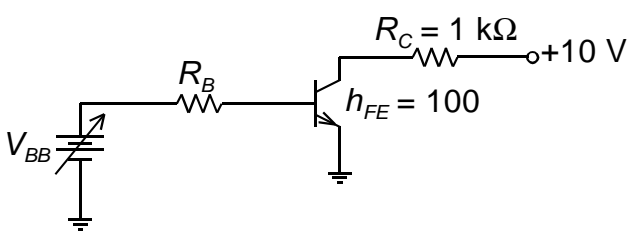


Fig. 242. BJT example.

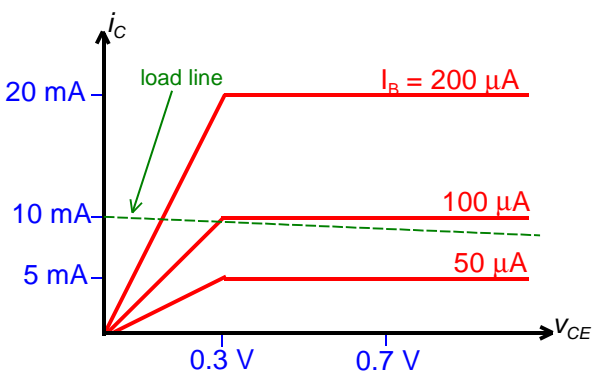


Fig. 243. Output characteristics.

I_B	I_{CM}	v_{CE}	R_S	Comments:
50 μA	5 mA	5 V	60 Ω	active region
93 μA	9.3 mA	0.7 V	32.3 Ω	edge of saturation
97 μA	9.7 mA	0.3 V	30.1 Ω	at corner
100 μA	10 mA	0.291 V	30 Ω	left of corner (see below)
200 μA	20 mA	0.148 V	15 Ω	left of corner

Example calculation for $I_B = 100 \mu\text{A}$:

$$v_{CE} = 10 \text{ V} \frac{R_S}{R_S + R_C} = 10 \text{ V} \frac{30 \Omega}{1\text{k}\Omega + 30 \Omega} = 0.291 \text{ V} \quad (286)$$

Rule of Thumb Voltages

Recall the typical assumptions detailed in the section on static diode characteristics:

$$v_{BE} < 0.65 \text{ V} \Rightarrow \text{cutoff}$$

$$v_{BE} = 0.70 \text{ V} \Rightarrow \text{active}$$

$$v_{BE} > 0.75 \text{ V} \Rightarrow \text{saturation}$$

Power Dissipation

The instantaneous collector power dissipation in a BJT is given by $p_C = v_{CE} i_C$. We note the following:

- Power dissipation is essentially zero in cutoff.
- Power dissipation is very small in saturation.
- Power dissipation is maximum at $v_{CE} = \frac{1}{2} V_{CC}$, $i_C = \frac{1}{2} V_{CC}/R_C$.

Inverse Mode

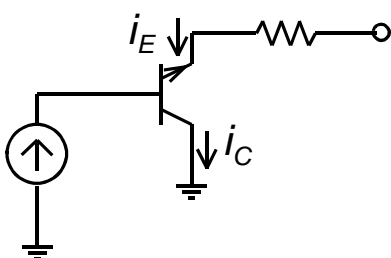


Fig. 244. Inverse BJT.

The collector and emitter terminals are not interchangeable, because the BJT is not constructed symmetrically. If we reverse these connections, we have:

$$i_E = h_{FC} i_B, \quad \text{where } h_{FC} \approx 0.1 \quad (287)$$

If i_B is large enough then the BJT operating point moves into the inverse saturation region, for which:

$$V_{EC \text{ sat - inverse mode}} \ll V_{CE \text{ sat - normal mode}} \quad (\text{typically } \approx 1 \text{ mV})$$

Switching into and out of inverse saturation is slower, thus this mode is used only in special applications (e.g., TTL input circuit).

Diode Switching Characteristics

Recall that a diode is a p-n junction.

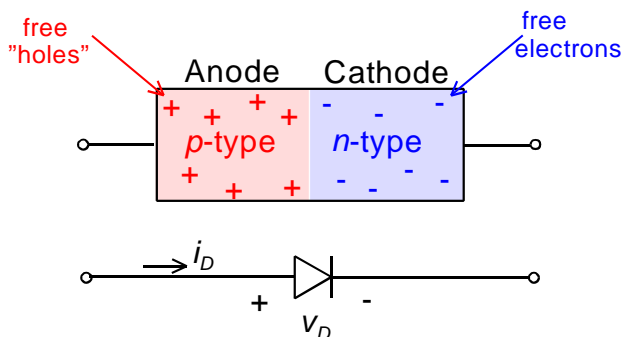


Fig. 245. Simple (abrupt) p-n junction.

In the *p-type* material:

- Holes, the majority carriers, are generated primarily from doping.
- Electrons, the minority carriers, are generated thermally.

In the *n-type* material:

- Electrons, the majority carriers, are generated primarily from doping.
- Holes, the minority carriers, are generated thermally.

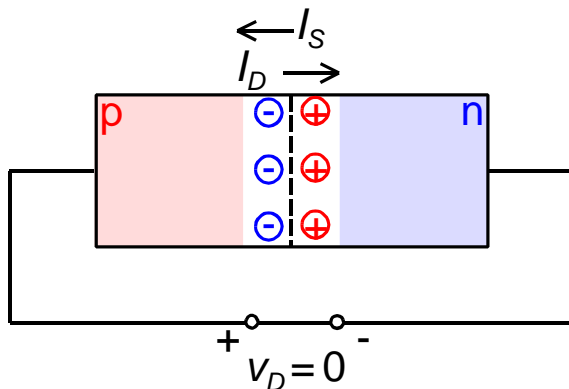


Fig. 246. p-n junction under zero bias, showing bound charges in the depletion region.

Zero Bias

Holes diffuse from the p-type material to the n-type material, where the hole density is lower.

Electrons diffuse from the n-type material to the p-type material, where the electron density is lower.

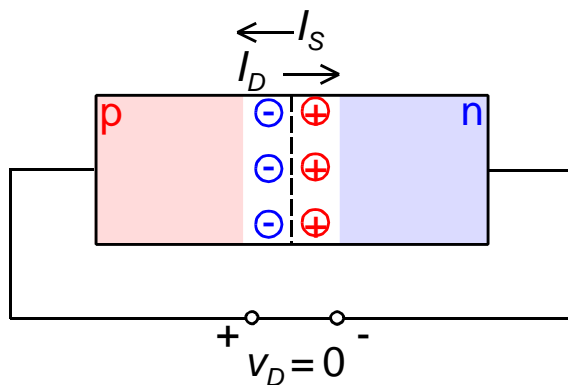


Fig. 247. *P-n* junction under zero bias, showing bound charges in the depletion region (Fig. 246 repeated).

The diffusion of the majority carriers gives rise to a diffusion current, I_D .

The diffusion current exposes bound charges in the vicinity of the junction. The region of bound charges is called the depletion region (because it is depleted of carriers).

The E field created by the bound charges opposes the flow of the diffusion current.

Thermally generated minority carriers will diffuse randomly to the depletion region where they are swept across the junction by the E field created by the bound charges, giving rise to a drift current, I_S .

At equilibrium, $I_D = I_S$, and net current is zero. The steady-state minority carrier distribution at equilibrium is shown below:

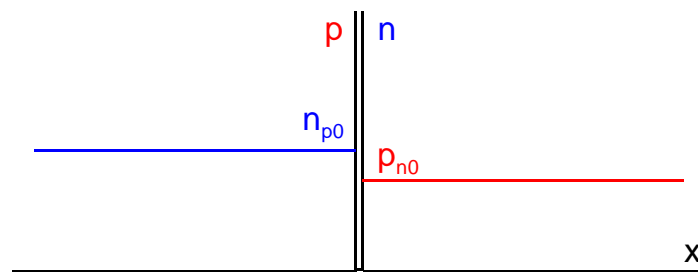


Fig. 248. Minority carrier distribution of an abrupt *p-n* junction under zero bias. The relative densities of n_{p0} and p_{n0} were chosen arbitrarily.

Reverse Bias

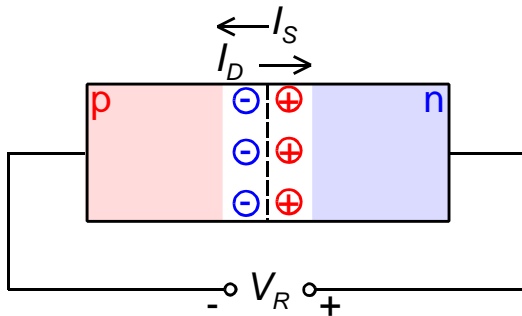


Fig. 249. Abrupt p - n junction under reverse bias.

The potential across the junction increases due to the applied reverse bias.

This causes more of the minority carriers to be swept across the junction.

In a sense the depletion region grows, but more insight is gained by looking at the minority carrier distribution:

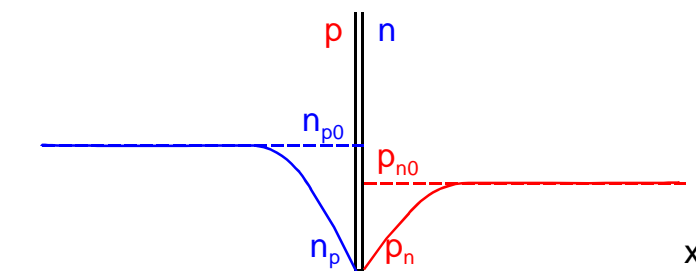


Fig. 250. Minority carrier distribution of reverse-biased abrupt p - n junction.

Because of this minority carrier distribution, minority carriers continue to diffuse toward the junction, thus the current I_S continues to flow.

However, the current I_D is essentially reduced to zero, because the increase in junction potential prevents diffusion of the majority carriers.

The resulting net current is just I_S , the reverse saturation current. This current is quite small because the minority carrier density is very low (remember, the minority carriers arise only from thermal generation).

Forward Bias

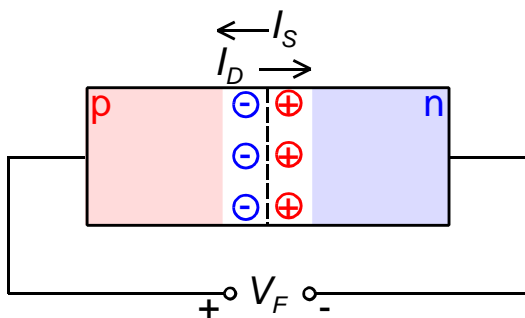


Fig. 251. Abrupt p - n junction under forward bias.

Applied forward bias decreases the junction potential from its value at zero bias.

This allows the majority carriers to diffuse across the junction, increasing the current I_D . This current can be quite large because of the number of majority carriers.

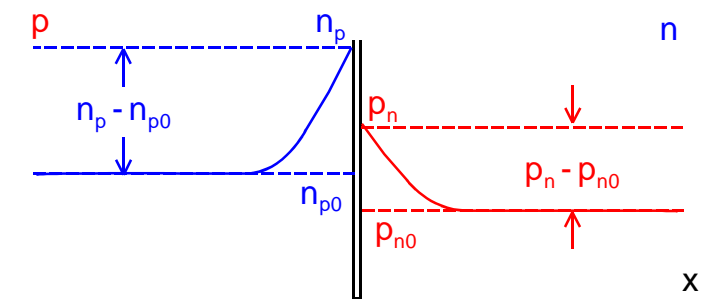


Fig. 252. Minority-carrier distribution of forward-biased abrupt p - n junction

Note, however, that when majority carriers cross the junction they become minority carriers.

The large number of carriers crossing the junction causes a tremendous increase in the minority carrier density, as shown.

Note also that the higher the forward current, the higher the minority carrier density at the junction. The excess minority carriers at the junction, $p_n - p_{n0}$, or $n_p - n_{p0}$, is called the stored charge.

Diode Switching

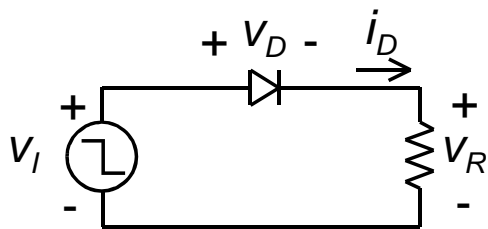


Fig. 253. Simple diode switching circuit.

Consider this simple diode circuit with the input voltage shown below. It is assumed that V_F and $|V_R|$ are much larger than the forward drop of the diode.

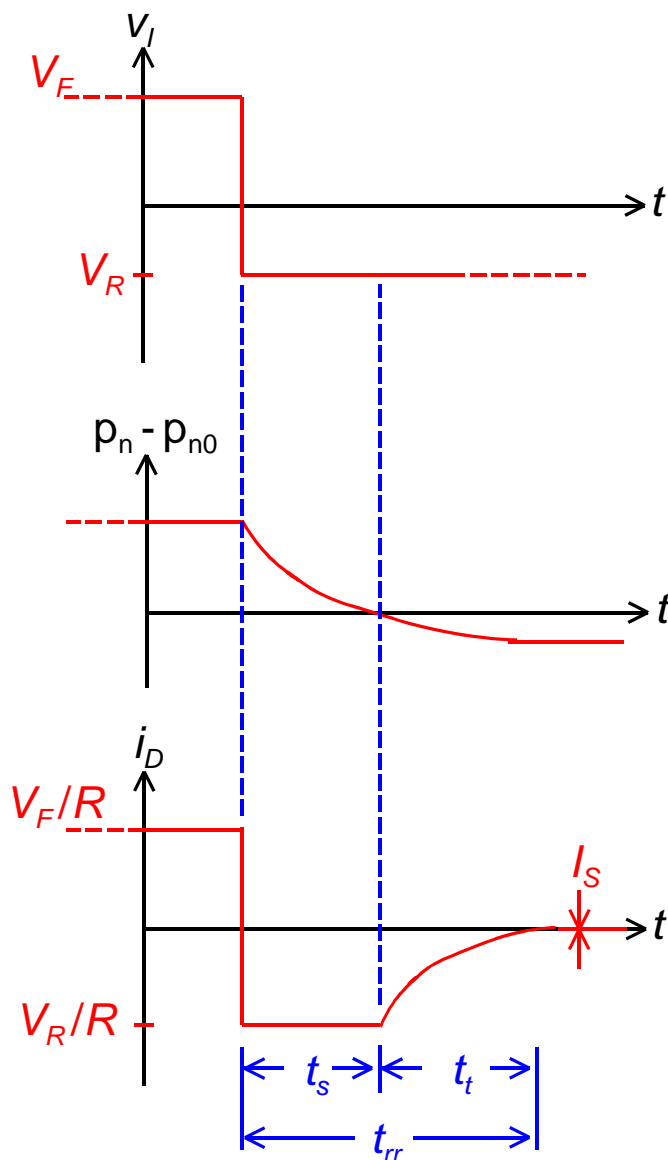


Fig. 254. Diode switching waveforms.

In the forward biased interval, the diode has a minority carrier density as shown in Fig. 252. The stored charge and the diode current as functions of time are shown at left.

When the voltage switches from V_F to V_R , the diode cannot perform as a reverse-biased diode until the minority carrier distribution returns to that shown for the reverse-biased case (Fig. 250).

This cannot happen instantaneously.

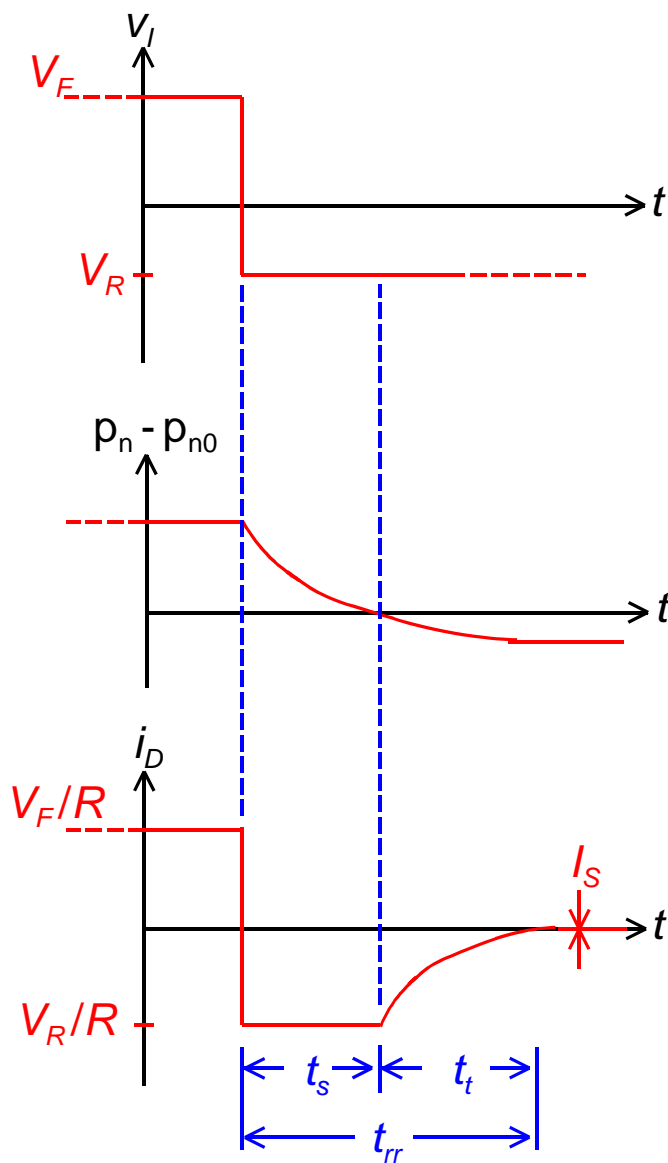


Fig. 255. Diode switching waveforms (Fig. 254 repeated).

In fact, because the forward biased minority carrier density at the junction is quite large, there can be a large reverse diode current, as shown.

The larger reverse current continues to flow until the stored charge is removed and the minority carrier density at the junction drops to the zero-bias level.

The time required for this to occur is called the storage time, t_s ; it is directly proportional to the forward current, I_F , and inversely proportional to the reverse current, I_R .

Storage time can be empirically described:

$$t_s \approx \tau_d \ln \left(1 + \frac{I_F}{I_R} \right) \quad (288)$$

where τ_d is a constant, characteristic of the particular diode.

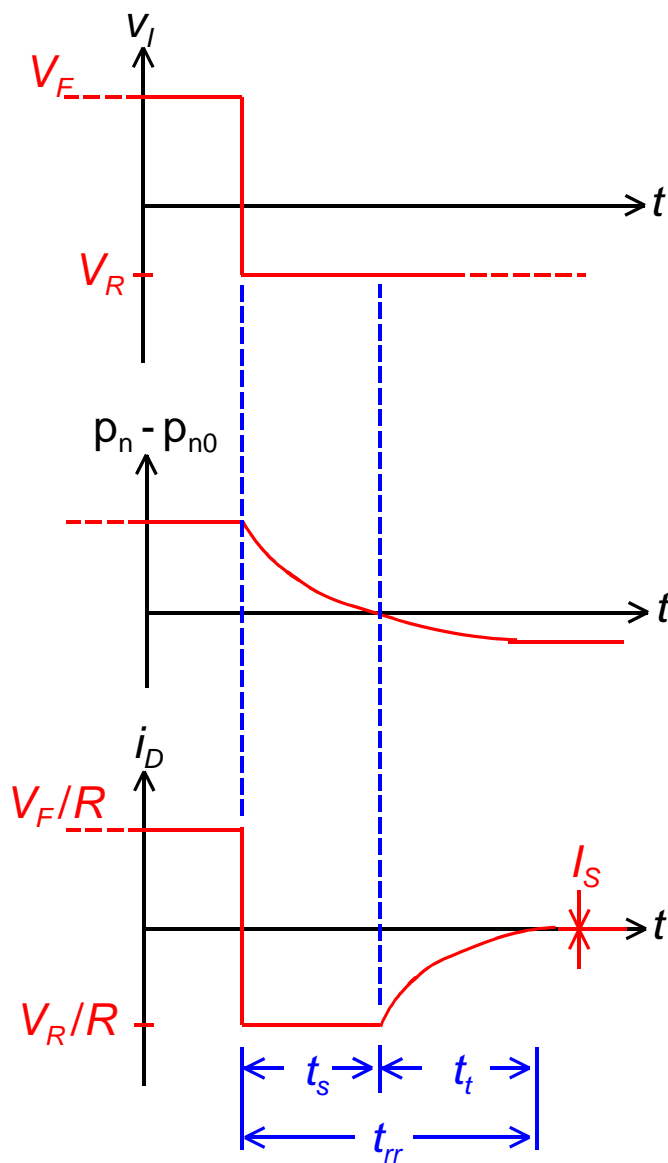


Fig. 256. Diode switching waveforms (Fig. 254 repeated).

After the stored charge has been removed, reverse current continues to flow, but decreases in magnitude until the minority carrier density at the junction drops to zero and the junction capacitance is charged through R to the voltage V_R .

This additional interval is called the transition time, t_t .

The total reverse recovery time is the sum of the storage time and the transition time:

$$t_{rr} = t_s + t_t \quad (289)$$

t_{rr} can be less than 1 ns in switching diodes, to as high as several μs in high-current diodes.

Schottky Diodes



Fig. 257. Schottky diode.

These diodes use a metal - n-type semiconductor junction.

The metal functions as p-type material. However, with applied forward bias, electrons flow into the metal where they are not minority carriers.

Thus, there is no stored charge and $t_s = 0$.

Typical total recovery times are 50 ps, and, for aluminum-on-silicon, the forward voltage is 0.35 V.

Drawbacks of Schottky diodes include increased reverse saturation current and low breakdown voltage.

BJT and FET Switching Characteristics

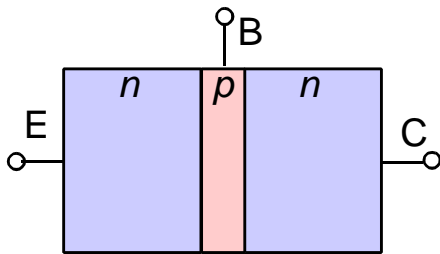


Fig. 258. Sandwich construction model of an *npn* BJT.

We first tackle switching characteristics of BJTs. An *npn* BJT is assumed to be the device in the descriptions that follow.

Recall the sandwich construction of the conceptual BJT:

Emitter \Rightarrow heavily doped n-type

Base \Rightarrow lightly doped p-type

Collector \Rightarrow lightly doped n-type

Actual devices are not constructed in this sandwich fashion, but this model serves us very well for the illustration of switching principles.

BJT Operation in the Active Region

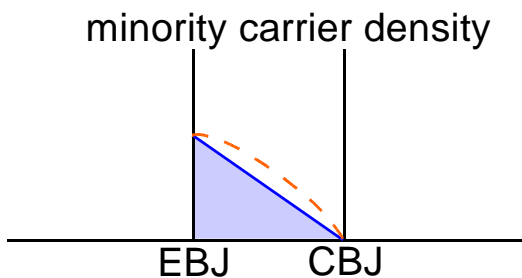


Fig. 259. Base-region minority-carrier density of BJT in active region.

The emitter-base junction (EBJ) is forward biased.

Electrons are injected from the emitter into the base, where they become minority carriers and diffuse toward the collector.

The minority carrier density in the base region is shown at left.

At the reverse-biased collector-base junction (CBJ) the electrons are swept into the collector producing collector current.

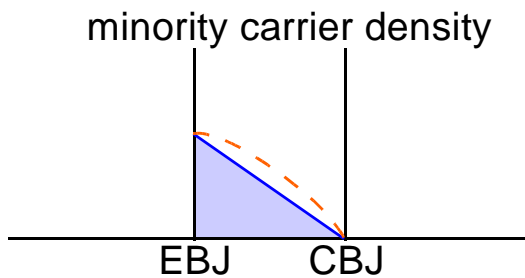


Fig. 260. Base-region minority-carrier density of BJT in active region (Fig. 259 repeated).

Because the base is lightly doped, the holes that are injected from the base into the emitter comprise a negligible part of the emitter current.

In addition, light base doping produces little recombination of the minority carriers in the base.

As a result, most of the injected electrons are allowed to reach the CBJ, resulting in $\alpha \approx 1$ and large β .

If we account for recombination in the base region, the minority carrier density is slightly bowed, as indicated by the dashed orange line in the figure.

It takes some time to set up this profile after forward bias is applied to the EBJ.

Upon removal of the forward bias, collector current will continue until the stored charge (the area under the curve) is removed.

BJT Operation in the Saturation Region

In saturation, the CBJ is also forward biased and additional stored charge is present in the base, as shown in the figure below.

This *excess stored charge* must be removed before collector current can cease. *Thus the switching speed of the device is significantly reduced.*

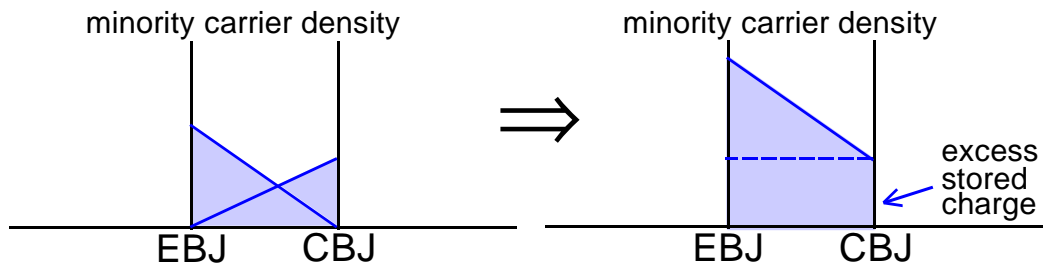


Fig. 261. Base-region minority-carrier density of a BJT in the saturation region.

Typical Switching Waveforms

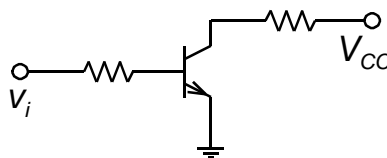


Fig. 262. Typical BJT switching circuit.

A simple BJT circuit driven with a pulse input yields the typical switching waveforms and definitions of intervals shown on the following page.

Study these waveforms carefully until you are familiar with all of the intervals that are defined.

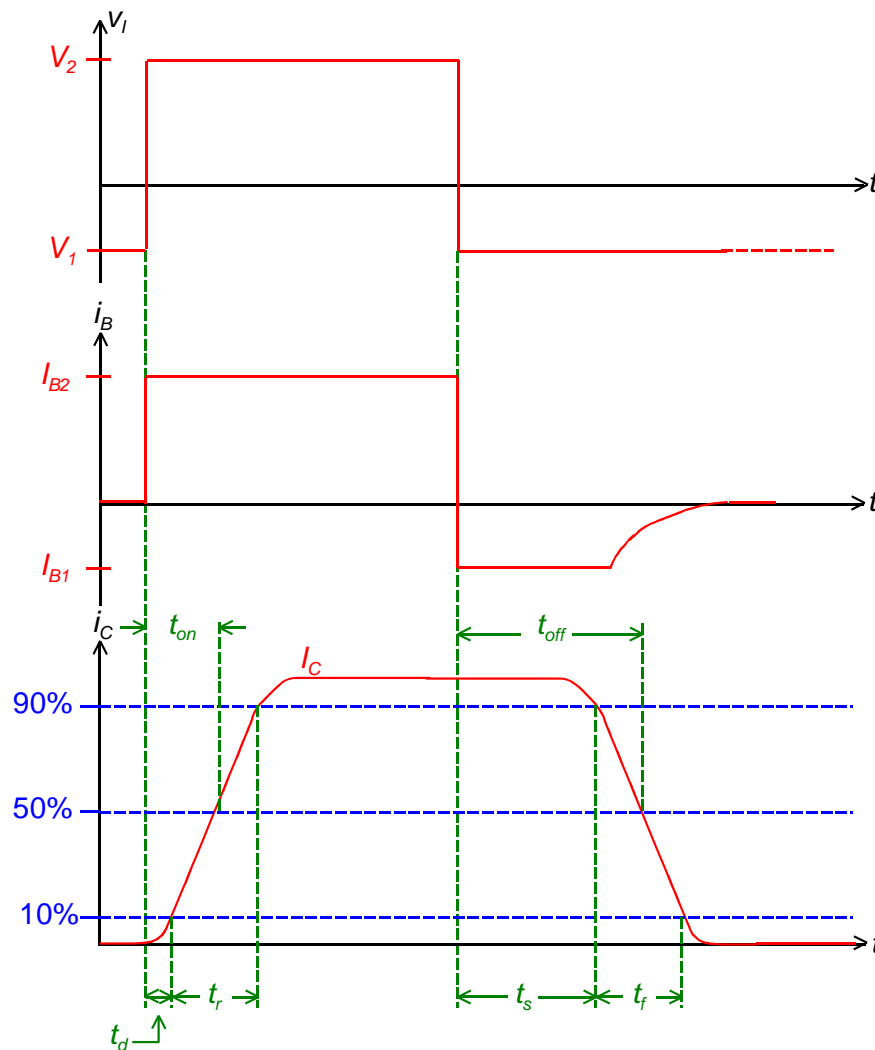


Fig. 263. Typical BJT switching waveforms.

t_{on} , turn-on time:

Δt from the + step change in i_B to the rising 50% I_C level.

t_{off} , turn-off time:

Δt from the - step change in i_B to the falling 50% I_C level.

t_d , delay time: Δt from the + step change in i_B to the 10% I_C level.

t_r , rise time: Δt from 10% I_C to 90% I_C .

t_s , storage time: Δt from the - step change in i_B to the 90% I_C level.

t_f , fall time: Δt from 90% I_C to 10% I_C .

Schottky Transistor

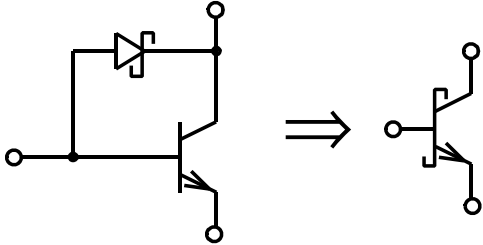


Fig. 264. Schottky transistor.

This bipolar junction transistor uses a Schottky diode between base and collector to prevent the collector from falling more than 0.35 V below the base.

Thus the transistor can never become heavily saturated.

Additional base current that would serve only to increase the excess stored charge is shunted through the diode to the collector.

The Schottky diode is easy to manufacture - the base metalization is merely extended over the collector region.

Increasing BJT Switching Speed

Because of the need to remove stored charge, the BJT behaves somewhat as a capacitor does. The addition of a speed-up capacitor as shown produces an RC attenuator circuit and increases switching speed:

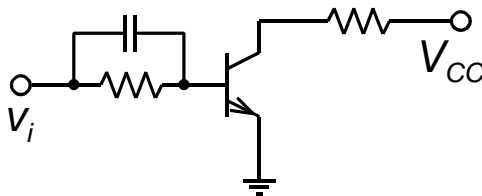


Fig. 265. Circuit to increase BJT switching speed.

FET Switching Characteristics

A field-effect transistor is a majority carrier device.

There are no minority carriers, no stored charge, and therefore, no storage time.

Speed limitations result from RC delays.

Low-power FETs have a high R_{on} and are generally slower than BJTs.

High-power FETs have a lower R_{on} and are generally faster than BJTs.

For a given FET, we can increase switching speed by reducing the load capacitance at the drain.

Introduction to DC-DC Conversion

The purpose of a dc-dc converter is to convert dc voltage from one level to another, at high efficiency, for the purpose of supplying power to a load.

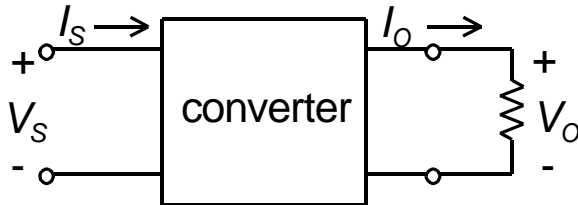


Fig. 266. Representative dc-dc converter system.

For the representative system at left, we can define input and output power, respectively:

$$P_S = V_S I_S \quad (290)$$

and

$$P_O = V_O I_O \quad (291)$$

We can also define the converter efficiency:

$$\eta = \frac{P_O}{P_S} = \frac{V_O I_O}{V_S I_S} \quad (292)$$

Converter efficiency is usually a function of I_O . In an ideal converter, input and output power are equal, i.e., the efficiency is 100%.

It is normally assumed that V_S and V_O are constant. In a well-designed converter this is almost true, though V_O usually contains a small ripple component.

Converter Basics

All converters use active devices or diodes as switches, and capacitors or inductors to store energy in electric or magnetic fields, respectively.

Capacitor-based converters use switches to transfer charge from one capacitor to another (and another, and another, etc.), and eventually to a load.

Salient features of capacitor-based converters include:

- Usually useful only at lower power levels.
- V_o depends on C and Q (remember $Q = CV$?).
- Higher switching frequencies reduce C required and also reduce output voltage ripple.

But switching losses (mostly active region dissipation during on-to-off and off-to-on transitions) are fixed per cycle, and increase with frequency.

- Typical switching frequencies are currently in the range of several hundred kHz to several MHz.

Inductor-based converters typically store energy in the magnetic field of one or more inductors, and use switches to transfer this energy to a capacitor (and a load) at the output. Features are:

- More efficient at higher power levels.
- Large energy storage requires high L values which, in turn, requires magnetic material for inductor cores.

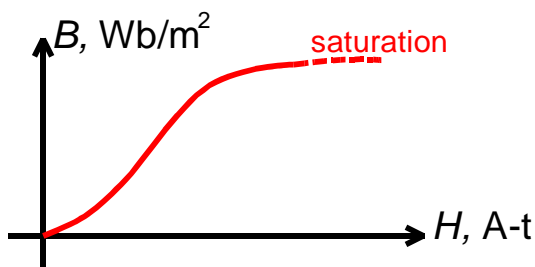


Fig. 267. Magnetization curve.

To reduce core losses and distortion of the internal switching waveforms, magnetic saturation of the core is avoided.

High output voltages require high inductor voltages, and from

$$V_L \propto f \Phi_{\max} = f A B_{\max} \quad (293)$$

small sizes (areas) imply higher switching frequencies, with the same increase in switching losses noted previously.

Capacitor-Based Converters

These are usually based on the *peak rectifier* and the diode *clamp* circuits.

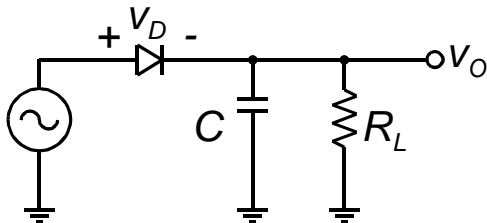


Fig. 268. Peak rectifier circuit.

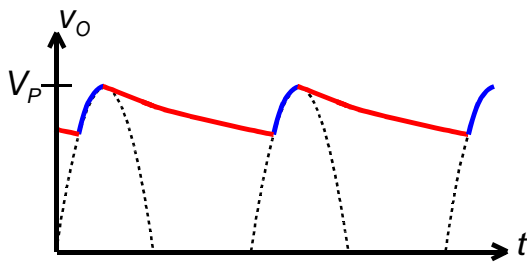


Fig. 269. Peak rectifier waveforms. Blue indicates when the diode carries forward current.

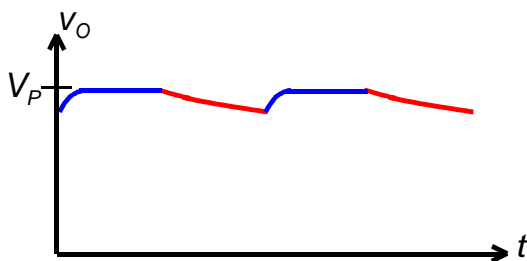


Fig. 270. Peak rectifier waveforms with square-wave input.

Peak Rectifier

Recall peak rectifier operation with a sinusoid:

- C charges to maximum input voltage, V_P , on positive half-cycle.
- C discharges through R_L throughout remainder of cycle.
- Diode forward current consists of one pulse per cycle.
- Output ripple is reduced with higher f and higher R_L .

Operating with a square-wave input:

- Increases the diode conduction angle.
- Reduces output ripple.
- Provides higher average output voltage.

As you might expect, we will operate our converter with square-wave (or rectangular-wave) inputs.

Clamp

Interchanging the positions of the diode and the capacitor in the peak rectifier circuit gives us a diode clamp:

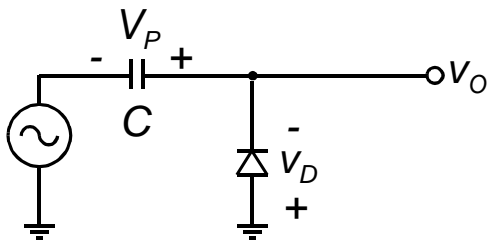


Fig. 271. Diode clamp circuit.
For convenience the clamp is left
unloaded.

Circuit operation:

- During the *first* negative half-cycle, the diode conducts.
- C charges to a maximum input voltage, V_P , with polarity shown.
- On all subsequent cycles, v_O equals the source voltage *plus* V_P .
- As a result, the output is clamped above zero.

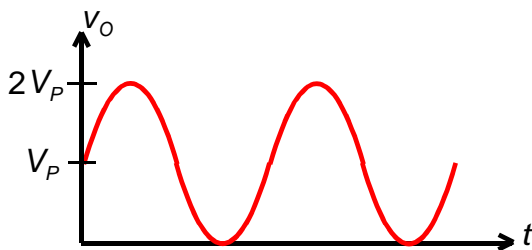


Fig. 272. Clamp circuit output voltage.

Also note:

- Connecting the anode of the diode to a voltage other than ground, clamps the output above *that* voltage.
- With a load attached, C discharges (slightly, if C is large) during each cycle, and is recharged at each negative peak of the input with a current pulse through the diode.
- Driving the clamp circuit with a square wave increases the diode conduction angle, and reduces the discharge of C with an attached load.

Building a Capacitor-Based Converter

We begin with a clamp, driven by a square wave, and follow that circuit with a peak rectifier:

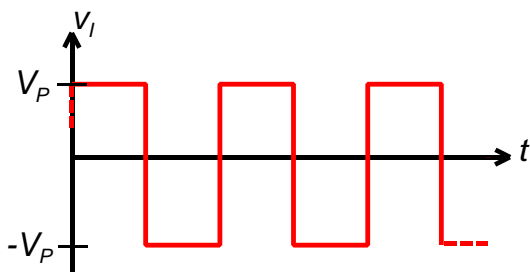


Fig. 273. Square-wave input to clamp + peak detector circuit.

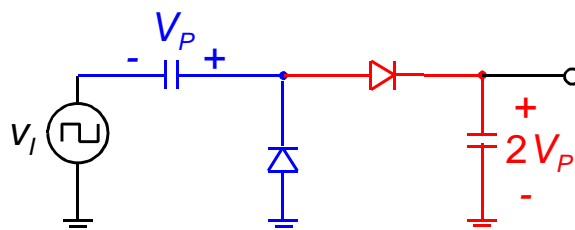


Fig. 274. Clamp followed by a peak detector. Steady-state capacitor voltages are noted in the figure.

Note that the dc output voltage is twice the input voltage magnitude. This circuit is called a voltage doubler.

We obtain the same output if we begin with a zero-to- V_P square wave, and clamp it above V_P volts:

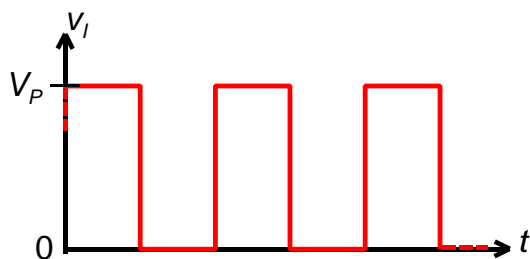


Fig. 275. Single-polarity square wave driving the doubler at right.

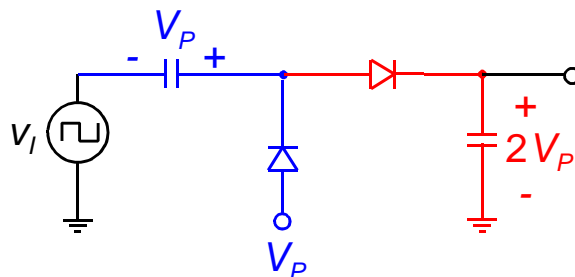


Fig. 276. Alternative voltage doubler circuit.

Normally, the square wave is derived from a dc supply (of V_P volts) using switches.

The single polarity square-wave is much easier to obtain, so the doubler circuit of Fig. 276 is preferred.

We continue to build our capacitor-based converter by adding another clamp circuit to the doubler of Fig. 276:

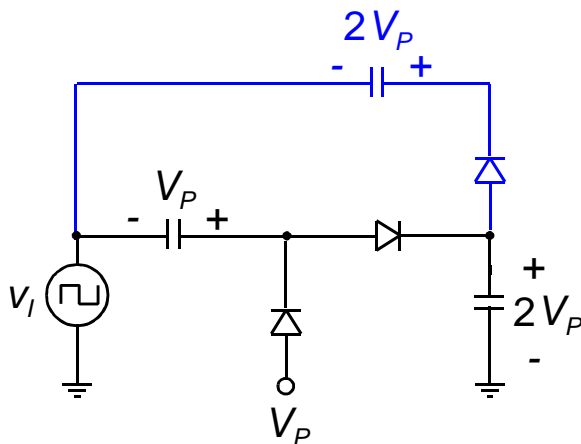


Fig. 277. Additional clamp added to the circuit of Fig. 276.

- The voltage reference for the second clamp is $2V_P$.
- The input square wave varies from zero to V_P .
- The capacitor of the second clamp charges to a dc voltage of $2V_P$.

Now we add another peak rectifier circuit:

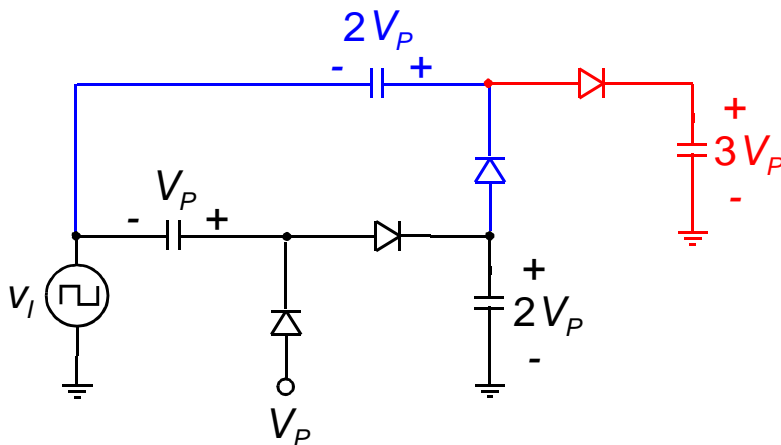


Fig. 278. Additional peak rectifier added to the circuit of Fig. 277.

- Note that now we have a dc output voltage of $3V_P$!!!
- We can continue with this process indefinitely (in theory).

We can redraw Fig. 278 in a more straightforward manner (on the following page . . .)

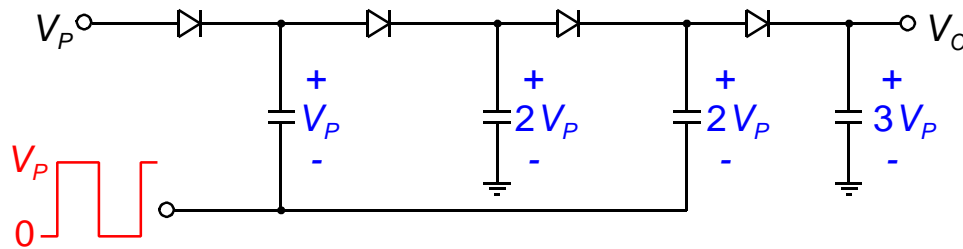


Fig. 279. Basic capacitor-based dc-dc converter. Capacitor voltages are steady-state values.

With the topology presented as above, the “bucket-brigade” nature of the circuit operation is more obvious.

We can reduce the number of stages needed by pulling the intermediate capacitors up to V_P when their neighbors are pulled to zero . . . this requires a second square wave, 180° out of phase with the first:

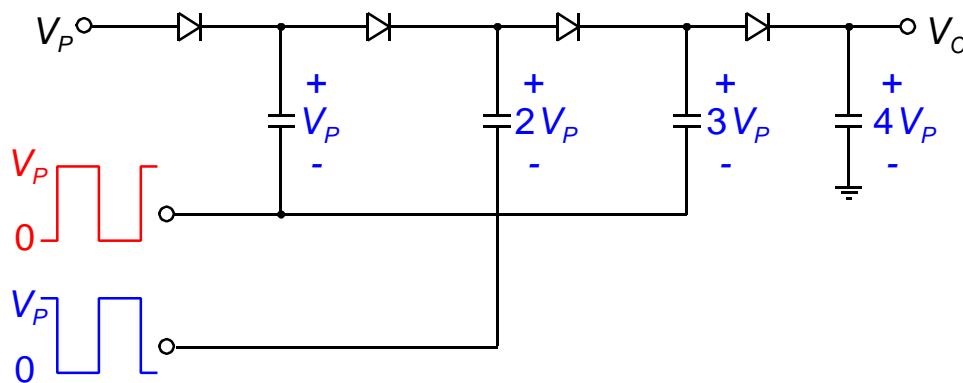


Fig. 280. Improved capacitor-based dc-dc converter. Capacitor voltages are steady-state values.

The generation of the square waveforms from the dc supply (V_P) is relatively easy. The reduced losses resulting from fewer stages usually makes this latter approach more attractive than the versions shown earlier in this section.

We can add more stages by alternating capacitor connections to the square wave sources:

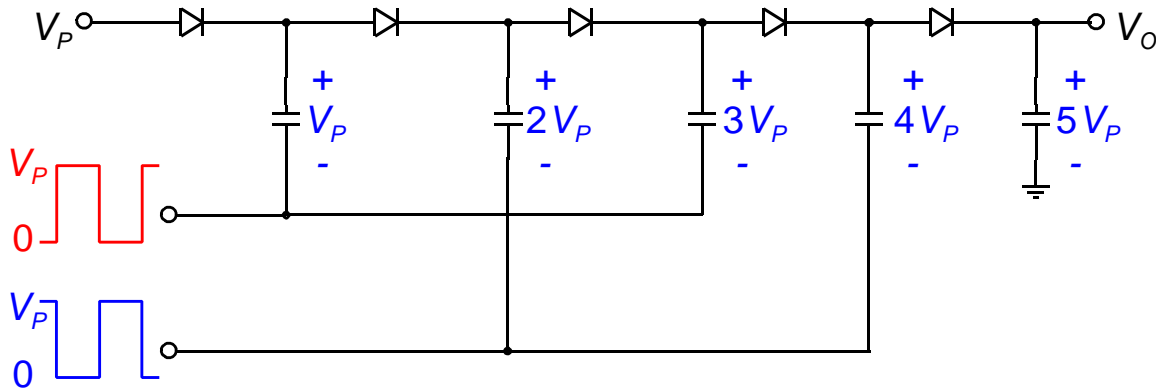


Fig. 281. Five-stage converter.

We can also generate negative voltages by reversing the diodes (and polarized capacitors such as electrolytics). Negative converters require one additional stage for an output magnitude equal to that of a corresponding positive converter.

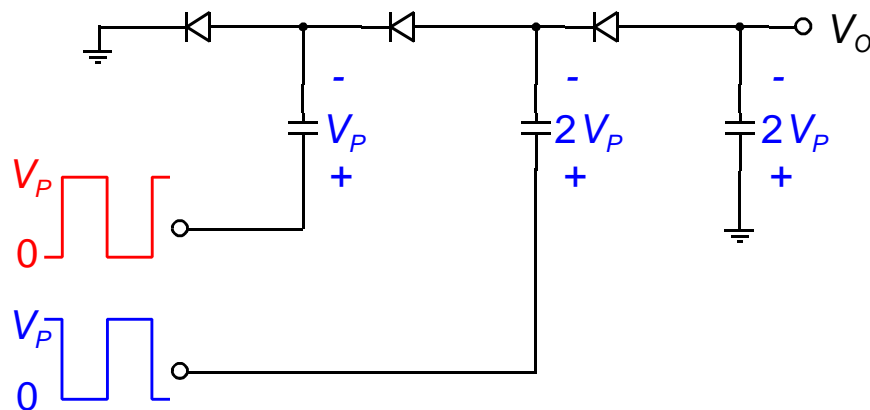


Fig. 282. Negative converter.

Nonideal Converters

- The dc output voltage is less than an integer multiple of the dc input voltage, due to the diode drop within each stage.

Schottky diodes reduce the effect of multiple diode drops.

- Additional voltage drops occur across the internal resistance of the square wave generators. These resistances should be kept as low as possible.

- Output ripple results from the discharge of the final capacitor through the load.

For a given load current, output ripple decreases as switching frequency (i.e., square-wave frequency) increases.

For a given frequency, output ripple decreases as load current decreases.

Simulation of a Four-Stage Converter

PSpice was used to simulate the four-stage converter shown below. Output voltages for various loads are shown on the following pages.

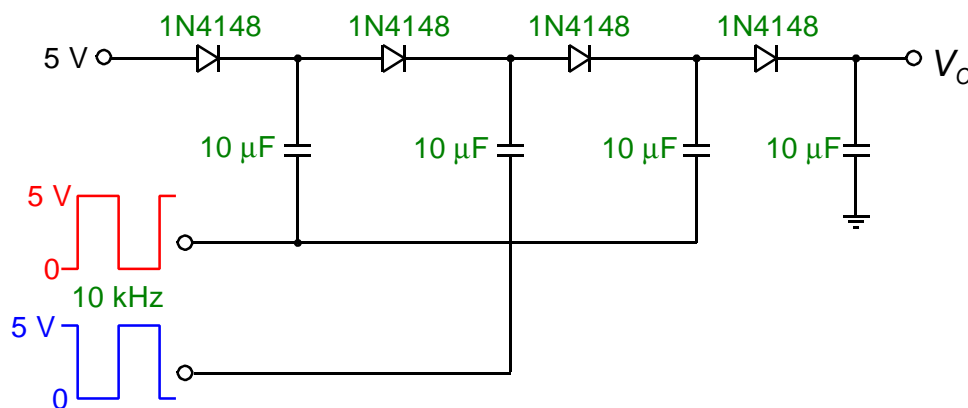


Fig. 283. The 4-stage converter circuit used for simulation. Piecewise-linear sources were used to simulate the square waves.

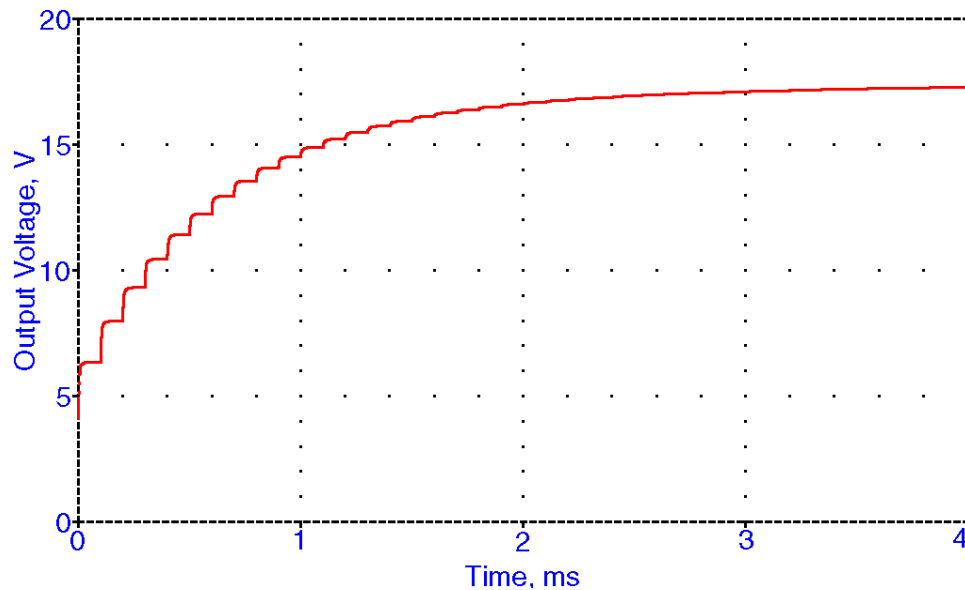


Fig. 284. Simulated no-load output voltage for four-stage converter. Note that the steady-state output voltage is less than the theoretical value, but has very little output ripple.

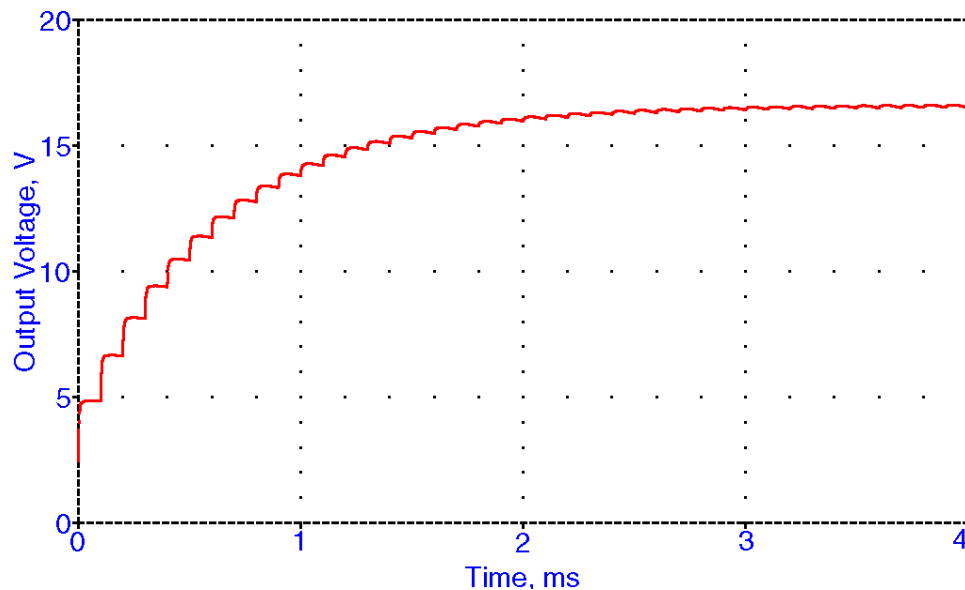


Fig. 285. Simulated output voltage, 1 k Ω load, for the four-stage converter. The steady-state output voltage has decreased, and output ripple has increased.

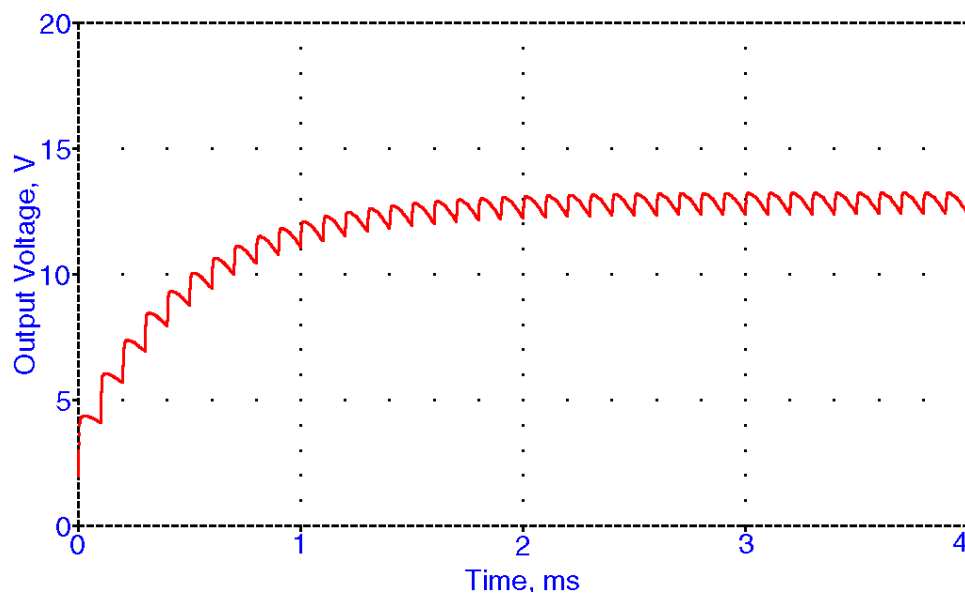


Fig. 286. Simulated output voltage, $100\ \Omega$ load, for the four-stage converter. With this heavy load, the steady-state output voltage has decreased significantly, and ripple has become quite large.

Inductor-Based Converters

There are three basic configurations of inductive converters:

- Buck Converter:

Output voltage is less than input voltage.

- Boost Converter:

Output voltage is greater than input voltage.

- Buck-Boost Converter:

Output voltage can be either greater or less than input voltage (in magnitude only, because as a consequence, the output voltage is negative).

Techniques and Assumptions for Inductive-Converter Analysis

- All elements are lossless (except for load resistance).
- Diode forward voltage is zero.
- In steady state (i.e., all waveforms are periodic)
- Output voltage is constant (negligible ripple voltage).

We will see that this is equivalent to the requirement that the output filter capacitor is infinitely large.

We will also see many *linear* inductor current waveforms, because we will often assume inductor voltages are constant. Note that:

$$\text{from } v_L = L \frac{di}{dt} \Rightarrow \frac{V_L}{L} = \frac{\Delta I_L}{\Delta t} \quad (294)$$

The latter equality merely describes the slope of the inductor current waveform.

Buck Converter

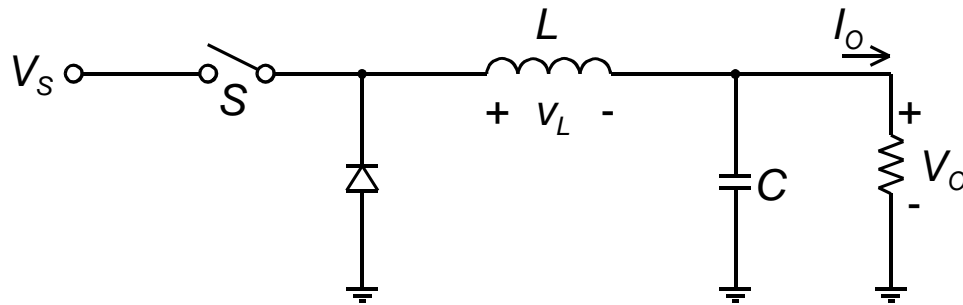


Fig. 287. Buck converter.

- S is implemented with an active device.
- The freewheeling diode provides a path for inductor current when the switch is open.

Switching Details:

We define:

t_c and t_o , the switch-closed and switch-open intervals,

T , the switching period,

and D , the switch duty ratio:

$$D = \frac{t_c}{T} \quad (295)$$

Thus, we can write:

$$t_c = DT \quad (296)$$

and, because $t_c + t_o = T$:

$$t_o = (1 - D)T \quad (297)$$

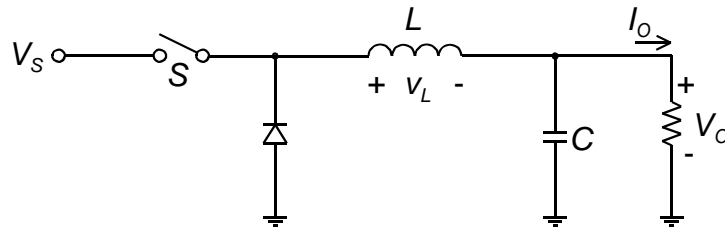


Fig. 288. Buck converter (Fig 287 repeated).

Inductor Current:

When the switch is closed:

$$v_L = V_S - V_O \quad (298)$$

So the inductor current increases linearly in this interval:

$$\frac{di_L}{dt} = \frac{V_S - V_O}{L} = \frac{\Delta I}{t_c} \quad (299)$$

When the switch is open:

$$v_L = -V_O \quad (300)$$

And the inductor current decreases linearly:

$$\frac{di_L}{dt} = \frac{-V_O}{L} = \frac{-\Delta I}{t_o} \quad (301)$$

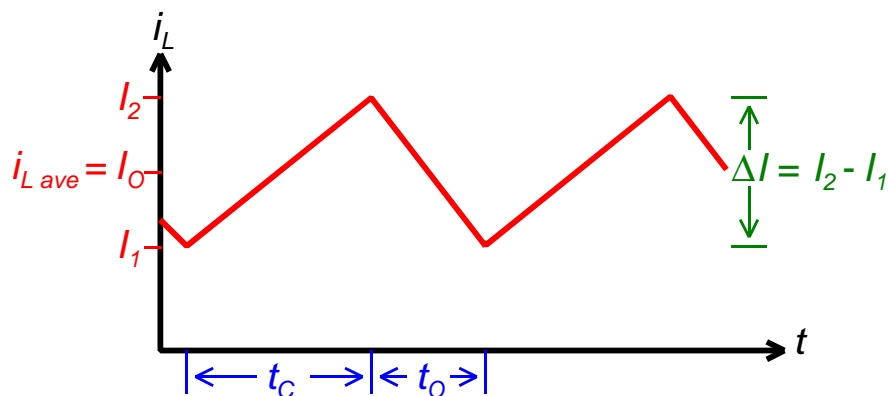


Fig. 289. Inductor current in the buck converter.

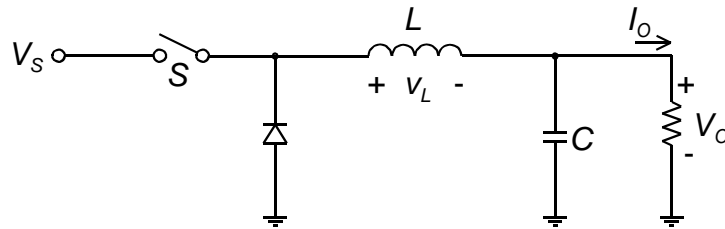


Fig. 290. Buck converter (Fig 287 repeated).

Output Current:

- The capacitor voltage can neither increase nor decrease.
- Therefore, the *average capacitor current is zero!!!*
- Therefore, the average inductor current must equal the average output current.

$$i_{L_{ave}} = I_o = \frac{I_1 + I_2}{2} \quad (302)$$

The variables in this equation are illustrated in Fig. 289.

Output Voltage:

First, we solve eq. (299) for ΔI :

$$\Delta I = \frac{(V_s - V_o)t_c}{L} = \frac{(V_s - V_o)DT}{L} \quad (303)$$

Now, we solving eq. (301) for ΔI :

$$\Delta I = \frac{V_o t_o}{L} = \frac{V_o (1 - D)T}{L} \quad (304)$$

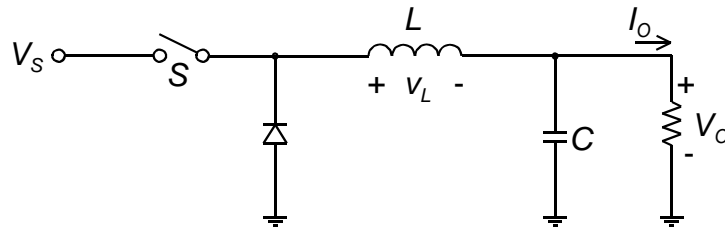


Fig. 291. Buck converter (Fig 287 repeated).

Recognizing the equality of eq. (303) and eq. (304) allows us to determine the output voltage:

$$\frac{(V_s - V_o)DT}{L} = \frac{V_o(1-D)T}{L} \Rightarrow (V_s - V_o)D = V_o(1-D) \quad (305)$$

from which:

$$DV_s = V_o \quad (306)$$

In a buck regulator, D is varied using feedback to regulate V_o .

Input Current:

Input current can be nonzero only when the switch is closed. It equals the inductor current in the switch-closed interval:

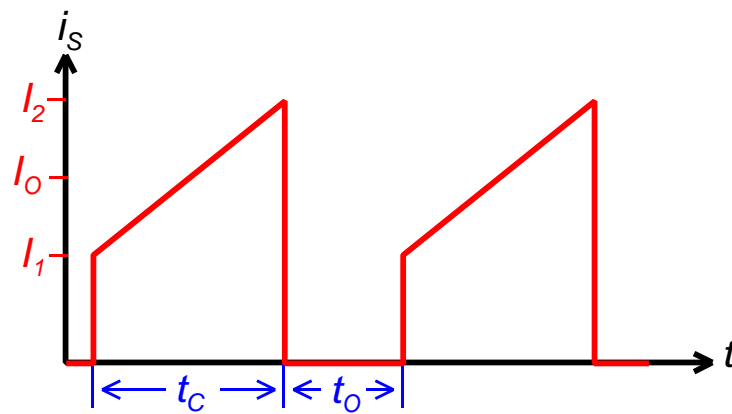


Fig. 292. Input current in the buck converter.

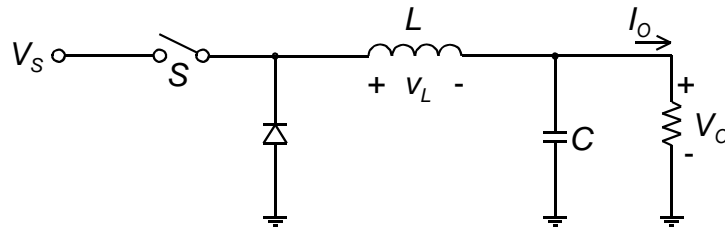


Fig. 293. Buck converter (Fig 287 repeated).

We can calculate the average input current:

$$i_{s_{ave}} = I_s = \frac{\text{area}}{T} = \frac{\frac{I_1 + I_2}{2} t_c}{T} = \frac{I_o t_c}{T} = DI_o \quad (307)$$

which can be written as

$$I_o = \frac{I_s}{D} \quad (308)$$

Input and Output Power:

We can determine average power with the average current values calculated previously:

$$P_o = V_o I_o = (DV_s) \left(\frac{I_s}{D} \right) = V_s I_s = P_s \quad (309)$$

This is consistent with our lossless assumption.

Real Buck Converters:

- Switch and diode have nonzero voltage drops when on.
- Switch, diode, inductor, and capacitor all have resistive losses. The equivalent series resistance (ESR) of the capacitor is very important, especially at high frequencies.

- Diode stored charge results in energy loss per cycle. As a result of these losses we have:

$$V_O < DV_S \quad I_S > DI_O \quad \text{and} \quad P_S > P_O$$

- Another phenomenon arises at light loads. First, let's recall the inductor current waveform:

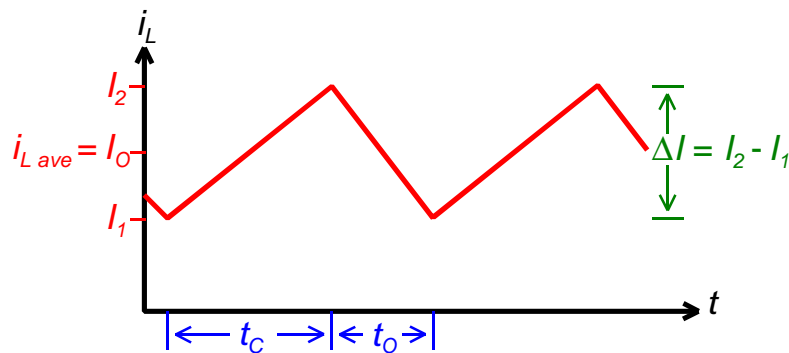


Fig. 294. Inductor current in the buck converter (Fig. 289 repeated).

- At low values of I_O , the minimum inductor current, I_1 , can fall to zero. Should I_O decrease further (i.e., less than $I_2/2$), the inductor current becomes discontinuous, and the model that we used to derive the converter equations becomes invalid.
- Operation of the buck converter with $I_1 \geq 0$ is called the continuous conduction mode.

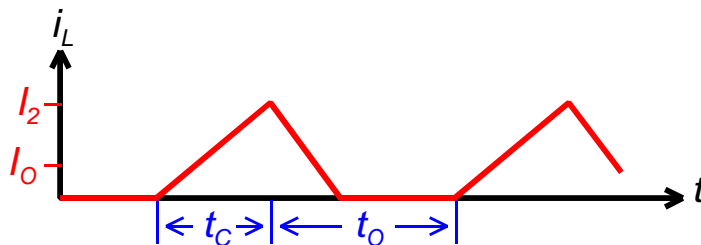


Fig. 295. Discontinuous-conduction mode inductor current in the buck converter.

In the discontinuous conduction mode the inductor current has three intervals per cycle, rather than two. A more complex model is required for circuit analysis.

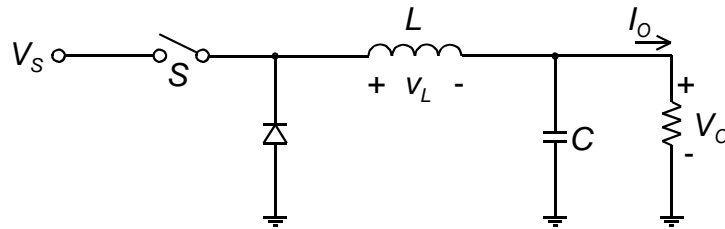


Fig. 296. Buck converter (Fig 287 repeated).

Estimating Peak-to-Peak Output Voltage Ripple:

Consider the following points:

- The steady-state output current is constant (because we assumed constant output voltage).
- In steady-state, the average capacitor current must be zero.
This is because the average (dc) output voltage neither increases nor decreases with time.
- From KCL we can write:

$$i_C = i_L - i_O \quad (310)$$

So we need only to shift the inductor current waveform down by I_O to obtain the capacitor current:

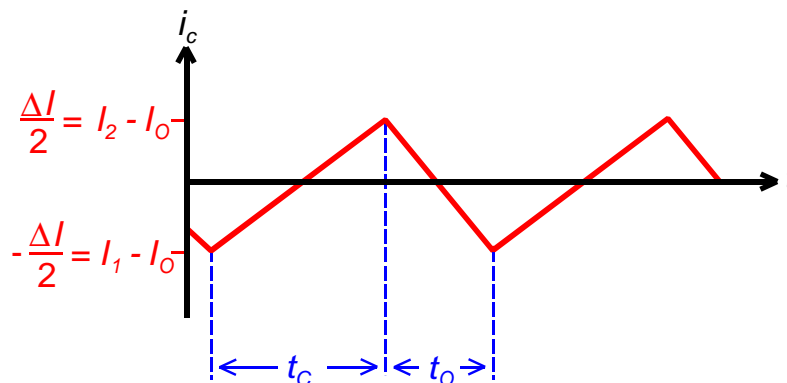


Fig. 297. Capacitor current in the buck converter.

- The capacitor current waveform of Fig. 297 indicates that V_o will not truly be constant, but will contain a ripple component described by:

$$v_o(t) = \frac{1}{C} \int_0^t i_c(t) dt + v_o(0) \quad (311)$$

- Thus, when i_c is greater than zero, v_o rises slightly above its average value of V_o . Conversely, when i_c is less than zero, v_o falls slightly below its average value of V_o .
- Because the output ripple is obtained by integrating linear current segments, the ripple waveform is made up of parabolic segments:

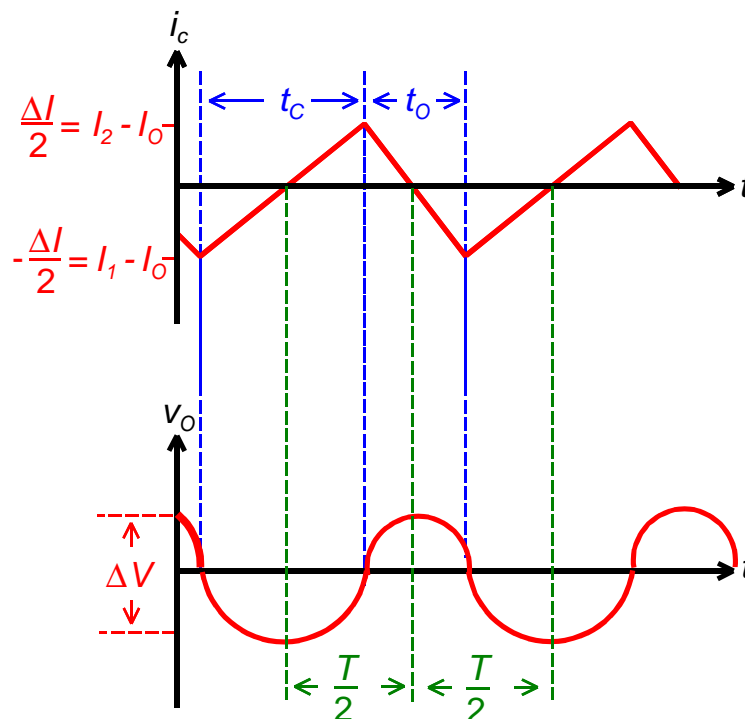


Fig. 298. The relationship between capacitor current and output voltage ripple in a buck converter.

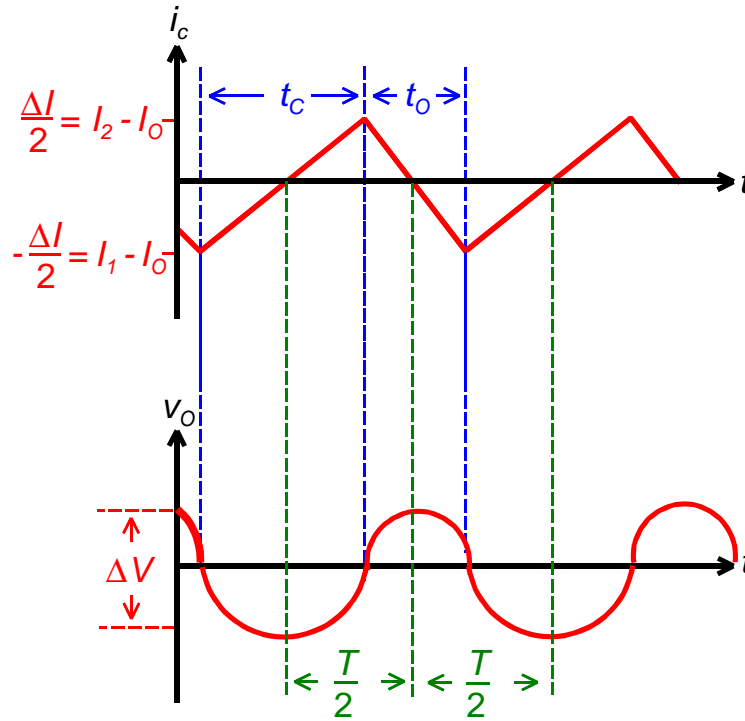


Fig. 299. The relationship between capacitor current and output voltage ripple in a buck converter (Fig. 298 repeated).

The change in output voltage ΔV results from the charge that is delivered to C during the interval when $i_c \geq 0$.

(Equivalently we could have equated ΔV with the charge taken from C when $i_c \leq 0$.)

The charge delivered is the area under a triangle with base and height equal to:

$$b = \frac{1}{2}t_c + \frac{1}{2}t_o = \frac{T}{2} \quad \text{and} \quad h = \frac{\Delta I}{2} \quad (312)$$

Thus:

$$\Delta Q = \frac{1}{2}bh = \frac{\Delta IT}{8} \quad \text{and} \quad \Delta V = \frac{\Delta Q}{C} = \frac{\Delta IT}{8C} \quad (313)$$

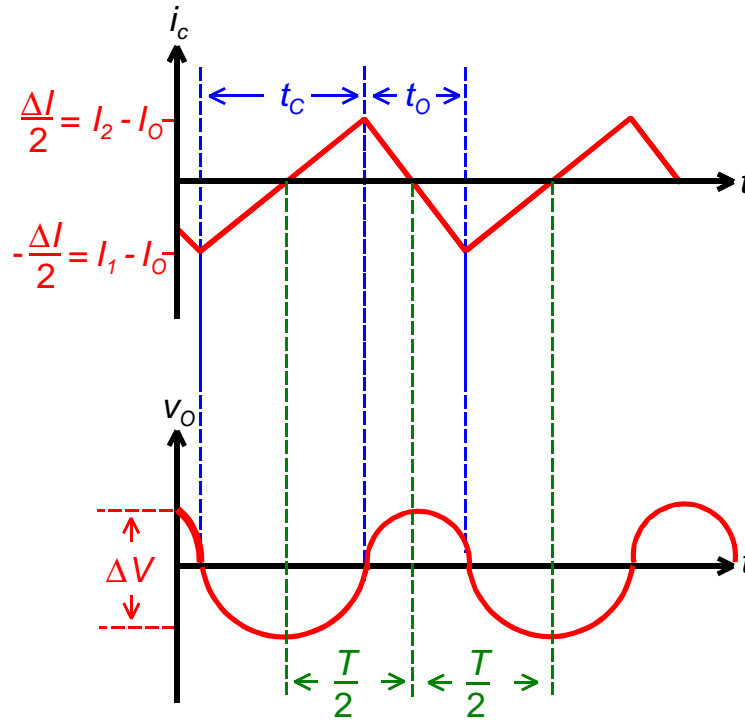


Fig. 300. The relationship between capacitor current and output voltage ripple in a buck converter (Fig. 298 repeated).

To complete our estimate we need to calculate ΔI . From eq.(301):

$$\Delta I = \frac{V_o}{L} t_o \quad (314)$$

But $V_o = DV_s$ and $t_o = (1-D)T$. Thus:

$$\Delta I = \frac{DV_s}{L} (1-D)T \quad (315)$$

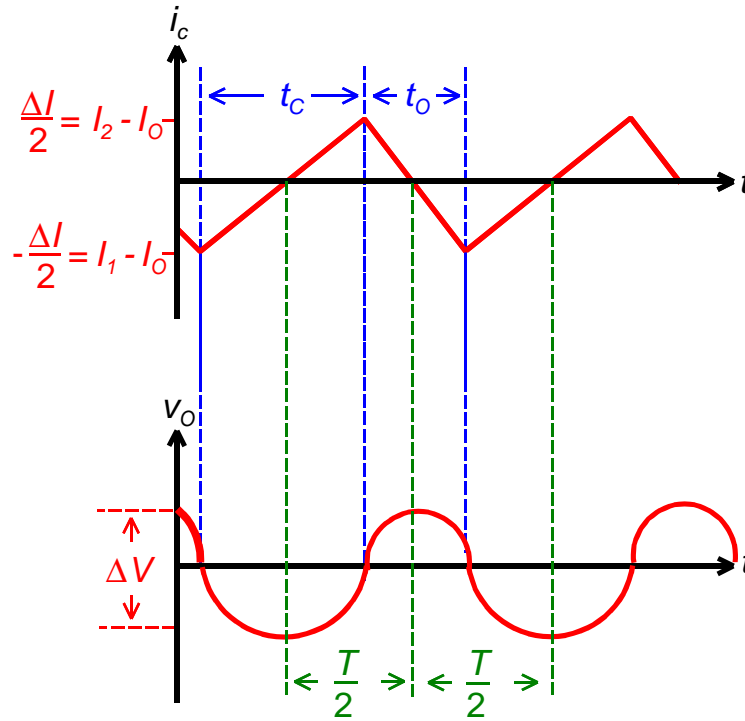


Fig. 301. The relationship between capacitor current and output voltage ripple in a buck converter (Fig. 298 repeated).

Finally, substituting eq.(315) into eq. (313) gives:

$$\Delta V = \frac{DV_s(1-D)T}{8LC} = \frac{V_s D(1-D)}{8f^2 LC} \quad (316)$$

We can show that this reaches a maximum at $D = 0.5$, from which we obtain an expression for the maximum ripple voltage:

$$\Delta V_{\max} = \frac{V_s}{32f^2 LC} \quad (317)$$

In the following example we shall see that there is another contribution to output ripple voltage - that due to the capacitor current flowing through the capacitor ESR.

Buck Converter Example

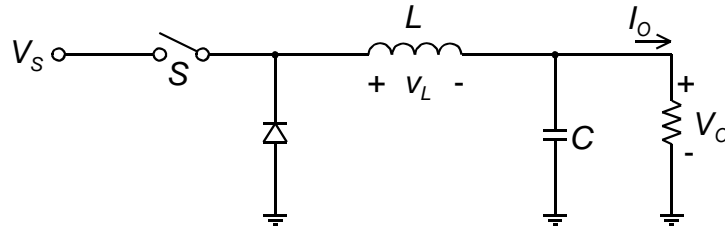


Fig. 302. Buck converter (Fig 287 repeated).

We will analyze a buck converter with the following:

$$V_S = 12 \text{ V} \quad L = 100 \text{ } \mu\text{H} \quad f = 25 \text{ kHz} \quad C = \text{assumed large}$$

The required output is 3 V at 1 A.

- First, we know that $T = 40 \text{ } \mu\text{s}$, and the required duty ratio is:

$$D = \frac{3 \text{ V}}{12 \text{ V}} = 0.25 \quad (318)$$

- From D , we can determine that $t_c = 10 \text{ } \mu\text{s}$ and $t_o = 30 \text{ } \mu\text{s}$.
- Note that an output of 3 V at 1 A corresponds to $R_{L \min} = 3 \text{ } \Omega$.
- From eq. (314):

$$\Delta I = \frac{V_o}{L} t_o = \frac{(3 \text{ V})(30 \times 10^{-6} \text{ s})}{100 \times 10^{-6} \text{ H}} = 0.9 \text{ A} = I_2 - I_1 \quad (319)$$

- And from eq. (302):

$$I_2 + I_1 = 2I_o = 2 \text{ A} \quad (320)$$

- Adding the two previous equations gives $2I_2 = 2.9 \text{ A}$, from which we obtain $I_2 = 1.45 \text{ A}$ and $I_1 = 0.55 \text{ A}$.

Now let's examine the output ripple voltage . . . suppose we have a capacitance of 1000 μF . From eq. (316):

$$\begin{aligned}\Delta V &= \frac{V_s D(1-D)}{8f^2 LC} \\ &= \frac{(12\text{ V})(0.25)(0.75)}{8(25 \times 10^3 \text{ Hz})^2 (100 \times 10^{-6} \text{ H})(10^{-3} \text{ F})} = 4.50\text{ mV}\end{aligned}\quad (321)$$

The calculated output ripple, 4.50 mV, is the value for our idealized circuit, but it is misleading . . . to see this we need to look at a typical filter capacitor.

- A Panasonic HFS, 1000 μF , 50 V capacitor:

Equivalent **S**eries **R**esistance (ESR) of 0.075 Ω .

Maximum allowable *rms* ripple current of 2.7 A.

- Our peak-to-peak ripple current, $I_2 - I_1$, flows through the capacitor ESR, producing a peak-to-peak ripple voltage of:

$$(0.9\text{ A})(0.075\Omega) = 67.5\text{ mV}\quad (322)$$

In this case, the ripple due to the drop across the capacitor ESR is much larger than that produced by charging the capacitor.

In every converter configuration we will examine, the output ripple voltage component due to capacitor ESR will completely dominate converter operation. The component due to charging the capacitor will be negligible.

(Note also that we are well within the capacitor current rating, so we need not be concerned with overheating the capacitor.)

Boost Converter

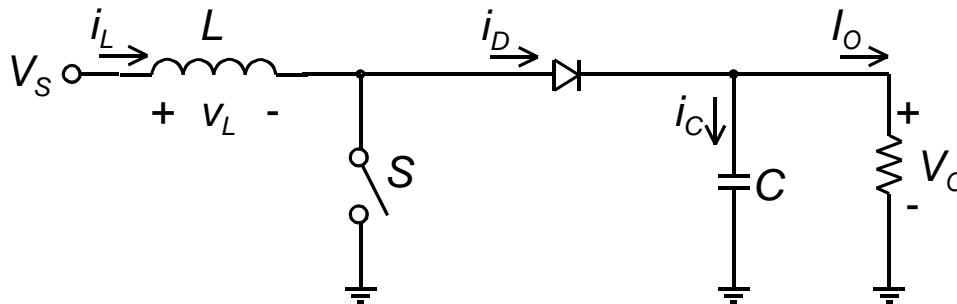


Fig. 303. Boost converter.

- Inductive energy stored when S is closed is transferred to the capacitor when S is open.
- Diode prevents C from discharging through S .

Inductor Current:

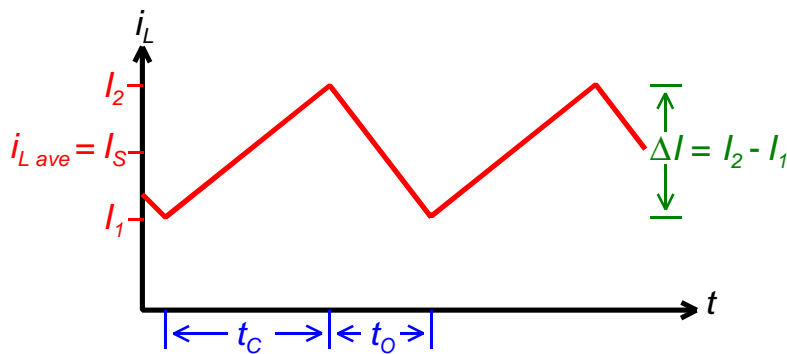


Fig. 304. Inductor current in boost converter.

- i_L increases when S closed, decreases when S is open:

S closed:

$$\frac{di_L}{dt} = \frac{V_S}{L} = \frac{\Delta I}{t_c} \quad (323)$$

S open:

$$\frac{di_L}{dt} = \frac{V_S - V_O}{L} = \frac{-\Delta I}{t_o} \quad (324)$$

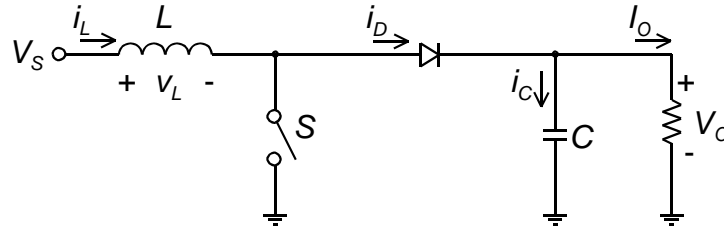


Fig. 305. Boost converter (Fig. 303 repeated).

Output Voltage:

We find the output voltage in exactly the same fashion as we did for the buck converter, i.e., we solve eqs. (323) and (324) for ΔI , and set them equal:

$$\Delta I = \frac{V_s t_c}{L} = \frac{(V_o - V_s) t_o}{L} \Rightarrow \frac{V_s D T}{L} = \frac{(V_o - V_s)(1 - D) T}{L} \quad (325)$$

from which:

$$V_s D = (V_o - V_s)(1 - D) = V_o - V_o D - V_s + V_s D \quad (326)$$

Solving yields:

$$V_o = \frac{V_s}{1 - D} \quad (327)$$

Input Current:

We know that the average input current, I_s , equals the average inductor current, I_{Lave} , and from our assumption of a lossless circuit:

$$V_o I_o = V_s I_s \Rightarrow I_o = \frac{V_s I_s}{V_o} = \frac{V_s I_s (1 - D)}{V_s} = I_s (1 - D) \quad (328)$$

$$\text{i.e., } I_o = I_s (1 - D)$$

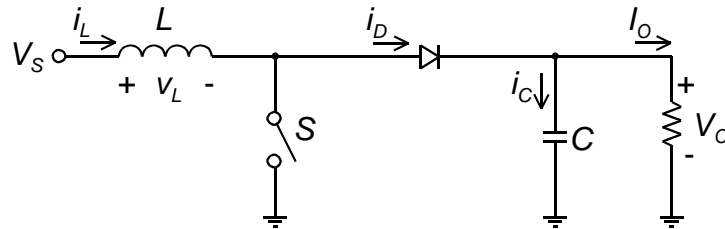


Fig. 306. Boost converter (Fig. 303 repeated).

Current Waveforms:

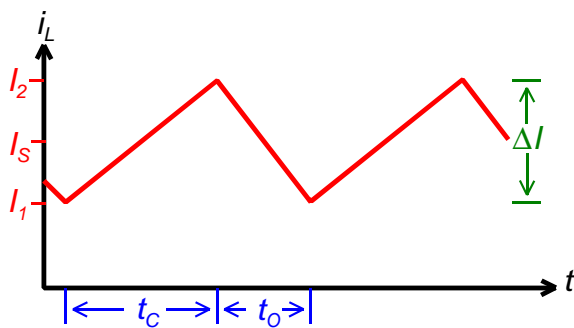
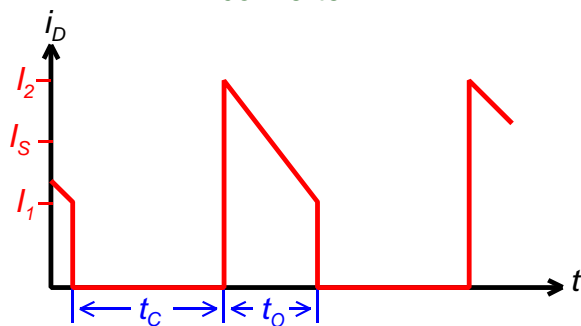


Fig. 307. Inductor current in boost converter.

ΔI is the peak-to-peak inductor ripple current. From eq. (323):

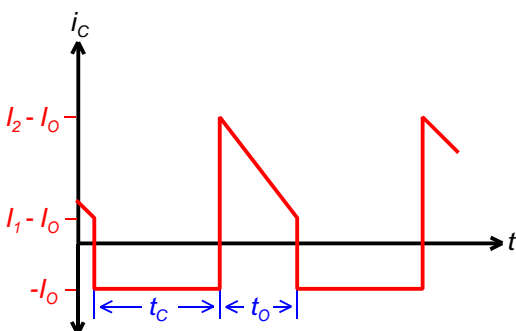
$$\Delta I = \frac{V_s}{L} t_c = \frac{V_s}{L} DT = \frac{DV_s}{fL} \quad (329)$$



The diode is reverse-biased when S is closed.

When S is open $i_L = i_D$.

Fig. 308. Diode current in boost converter.



From $i_C = i_D - I_o$, and because we've assumed I_o is constant, we obtain the waveform at left.

We use this waveform to find the output ripple voltage.

Fig. 309. Capacitor current in boost converter.

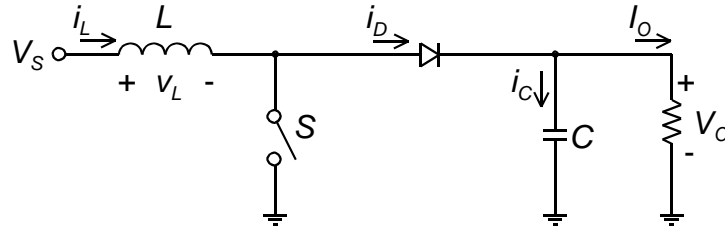


Fig. 310. Boost converter (Fig. 303 repeated).

Estimating Peak-to-Peak Output Voltage Ripple:

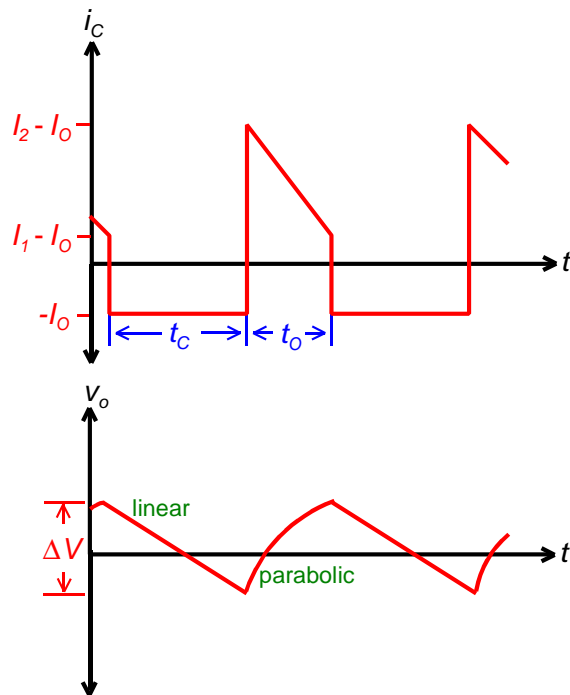


Fig. 311. Relationship between capacitor current and output voltage ripple in a boost converter.

We first concentrate on the ripple component resulting from charging the capacitor, and ignore that from the voltage drop across the capacitor ESR.

We will use the linear region shown in the figure to determine ΔV . From:

$$i = C \frac{dv}{dt} \quad (330)$$

we have:

$$I_o = C \frac{\Delta V}{t_c} = \frac{C \Delta V}{DT} \quad (331)$$

from which:

$$\Delta V = \frac{I_o DT}{C} = \frac{V_o DT}{RC} = \frac{V_o D}{fRC} \quad (332)$$

This peak-to-peak output ripple component is usually written in normalized fashion:

$$\frac{\Delta V}{V_o} = \frac{D}{fRC} \quad (333)$$

Output Voltage Sensitivity:

From:

$$V_o = \frac{V_s}{(1-D)} \quad (334)$$

we can see that the output voltage becomes very sensitive to small changes in duty ratio as D becomes large. This is illustrated in the figure below.

As a result of this sensitivity, operation of a boost converter at large duty ratios is generally avoided.

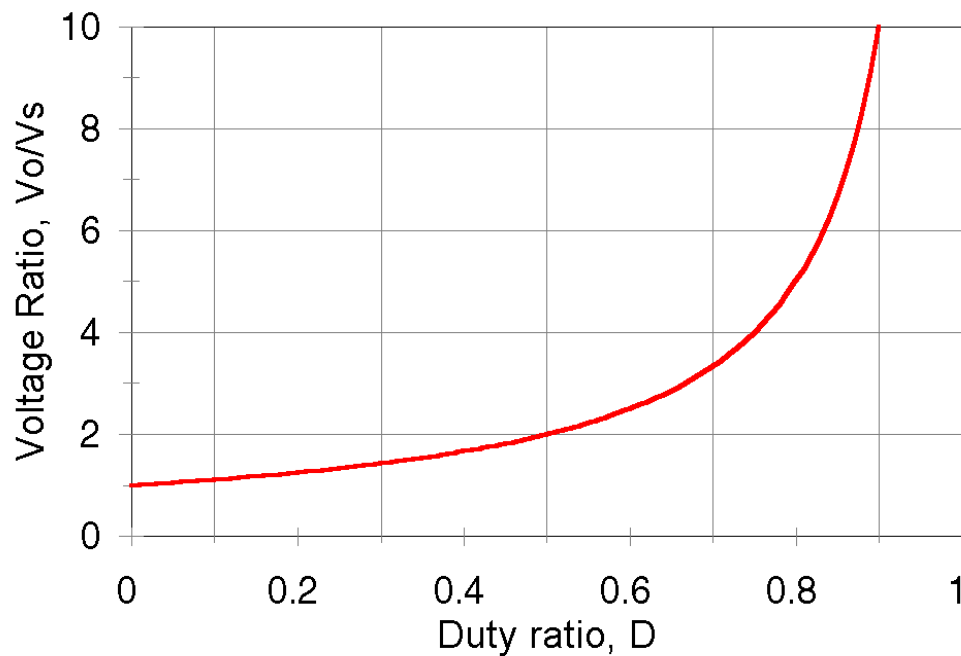


Fig. 312. Normalized output voltage vs. duty ratio for a boost converter.

Boost Converter Example

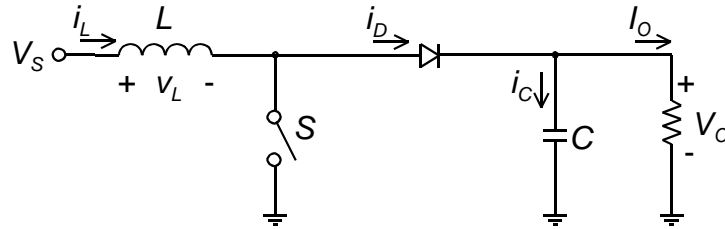


Fig. 313. Boost converter (Fig. 303 repeated).

We will analyze a boost converter with the following:

$$V_S = 5 \text{ V} \quad \text{and} \quad f_{\text{switch}} \approx 250 \text{ kHz}$$

We require:

$$V_O = 12 \text{ V} \quad I_{O \max} = 1 \text{ A} \quad i_{L \max} = 3.0 \text{ A} \quad \text{minimum ripple}$$

- From $V_O = \frac{V_S}{(1-D)}$, we obtain $D = 0.583$.
- Assuming a lossless circuit, the maximum source current is:

$$I_S = \frac{I_O}{(1-D)} = \frac{1 \text{ A}}{(1-0.583)} = 2.4 \text{ A} \quad (335)$$

- Now, from:

$$i_{L \max} = I_S + \frac{\Delta I}{2} \quad (336)$$

we obtain:

$$\Delta I = 2(i_{L \max} - I_S) = 2(3 \text{ A} - 2.4 \text{ A}) = 1.2 \text{ A} \quad (337)$$

- And, from:

$$\Delta I = \frac{DV_s}{fL} \quad (338)$$

we obtain:

$$L = \frac{DV_s}{f\Delta I} = \frac{(0.583)(5\text{ V})}{(250 \times 10^3)(1.2\text{ A})} = 9.72\text{ }\mu\text{H} \quad (339)$$

Note that this inductance value is *quite* small . . .

- Now, the peak-to-peak output ripple voltage due to i_C charging and discharging C is a different waveform than the ripple due to i_C flowing through the capacitor ESR.

Also, the peaks of these two waveforms do not occur at the same time.

As a result the total ripple voltage will be less than the direct sum of these two terms.

- We will assume that the direct sum is a worst case value, and use the Sprague Type 550D line of solid tantalum electrolytic capacitors (www.vishay.com).

At 20 WVDC (**W**orking **V**olts **DC**) the largest capacitance in this line is 100 μF , with an ESR of 0.075 Ω .

- The peak-to-peak output ripple voltage due to i_C charging and discharging C is:

$$\begin{aligned} \Delta V &= \frac{DV_o}{fRC} \\ &= \frac{(0.583)(12\text{ V})}{(250 \times 10^3\text{ Hz})(12\Omega)(100 \times 10^{-6}\text{ F})} = 23.3\text{ mV} \end{aligned} \quad (340)$$

- The peak-to-peak capacitor current (see, for example, Fig. 311) is just I_2 , which is the same as $i_{L\max}$, i.e., 3 A.

The peak-to-peak output ripple voltage due to this current is:

$$(3\text{ A})(0.075\Omega) = 225\text{ mV} \quad (341)$$

- Clearly, the contribution due to capacitor ESR dominates. We can improve this somewhat by choosing a larger inductor, which will reduce the peak-to-peak capacitor current.

For example, if we increase the inductance to 100 μH (approximately a factor of 10), the peak-to-peak capacitor current is 2.46 A, and the peak-to-peak ripple due to the capacitor current is reduced to 184 mV.

However, because the average inductor current is 2.4 A, a further increase in L does little to further reduce the ripple.

Before we leave this example, let us note again that the output ripple is dominated by the drop across the capacitor ESR. The other ripple component is, at best, small, and perhaps even negligible.

Buck-Boost Converter

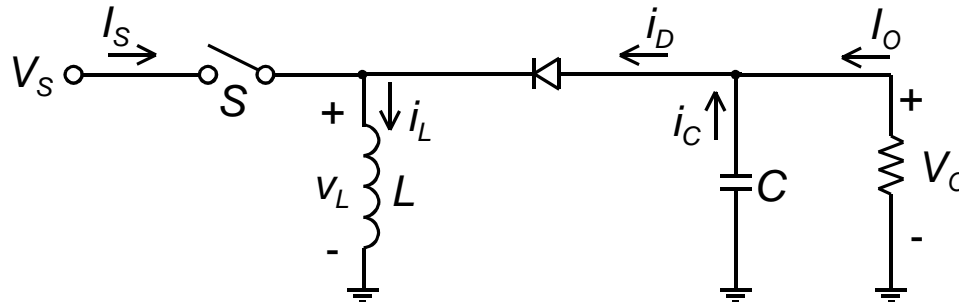


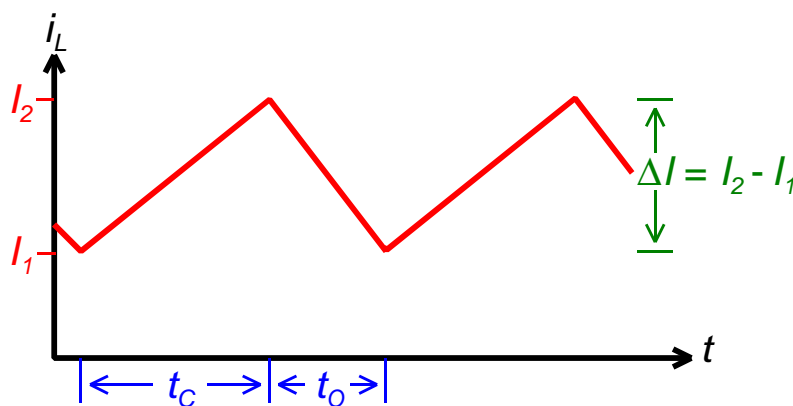
Fig. 314. The buck-boost converter, also called a *flyback* converter, or an *inverting* converter.

- Inductive energy is stored when S is closed, and transferred to C when S is open.
- Note that C never “sees” the source V_S directly, i.e., steady-state V_O is zero for either switch position.

Thus whether the circuit operates in *buck* or *boost* mode is determined solely by the energy stored in L (i.e., dependent upon D).

- Note also that V_O is *negative*.

Inductor Current:



S closed:

$$\frac{V_S}{L} = \frac{\Delta I}{t_c} \quad (342)$$

S open:

$$\frac{V_O}{L} = \frac{-\Delta I}{t_o} \quad (343)$$

Fig. 315. Inductor current in a buck-boost converter.

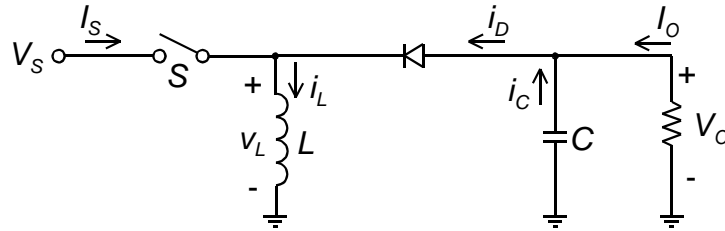


Fig. 316. Buck-boost converter (Fig. 314 repeated)

Output Voltage:

Solving eqs. (342) and (343) for ΔI and equating allows us to determine the output voltage:

$$\Delta I = \frac{V_s t_c}{L} = \frac{-V_o t_o}{L} \Rightarrow \frac{V_s D T}{L} = \frac{-V_o (1-D) T}{L} \quad (344)$$

from which:

$$V_s D = -V_o (1-D) \Rightarrow V_o = -V_s \left(\frac{D}{1-D} \right) \quad (345)$$

Notice that the dividing line between buck operation and boost operation occurs for $D = 0.5$.

Current waveforms are shown on the following page.

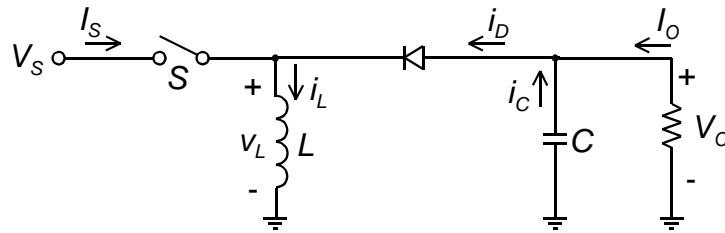


Fig. 317. Buck-boost converter (Fig. 314 repeated)

Current Waveforms:

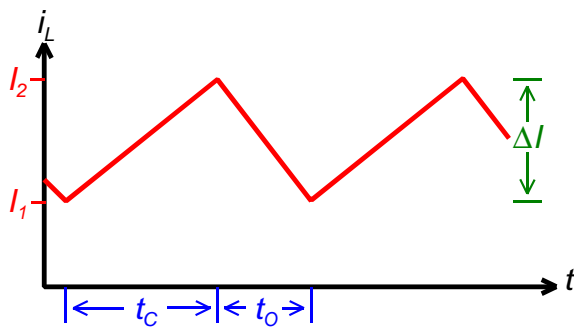


Fig. 318. Inductor current.

Peak-to-peak inductor ripple current:

$$\Delta I = \frac{V_s t_c}{L} = \frac{V_s D}{fL} \quad (346)$$

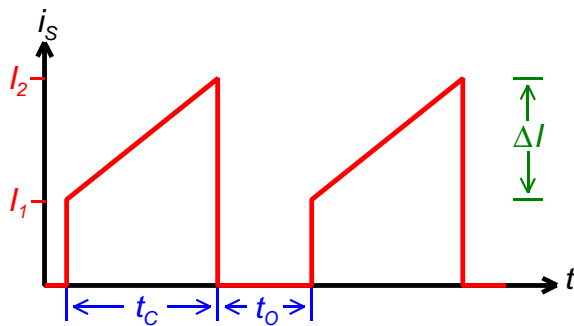


Fig. 319. Input current.

Dc input and output current are related by equating P_o and P_s :

$$V_o I_o = -V_s \left(\frac{D}{1-D} \right) I_o = V_s I_s \quad (347)$$

from which:

$$I_o = \left(\frac{1-D}{D} \right) I_s \quad (348)$$

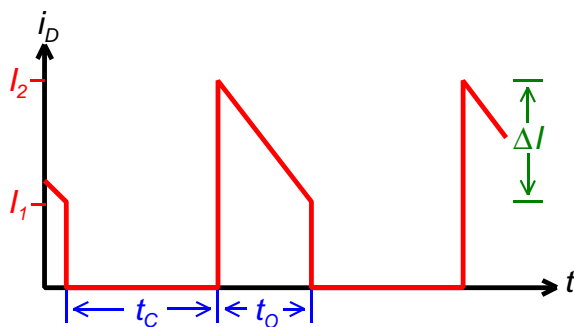


Fig. 320. Diode current.

This equation could also be derived by noting that $I_o = i_{D\text{ave}}$ and $I_s = i_{S\text{ave}}$.

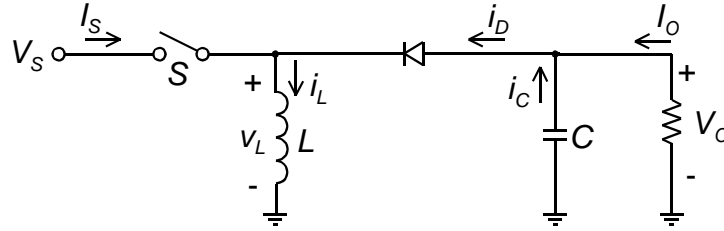


Fig. 321. Buck-boost converter (Fig. 314 repeated)

Estimating Peak-to-Peak Output Voltage Ripple:

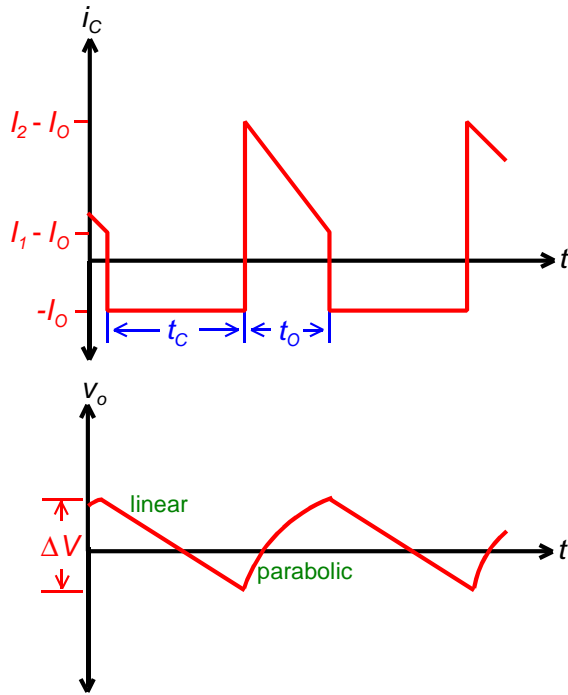


Fig. 322. Relationship between capacitor current and output voltage ripple in a buck-boost converter.

This development is identical to that for the boost converter. Again we concentrate on the ripple component resulting from charging the capacitor, and ignore that from the voltage drop across the capacitor ESR.

From:

$$i = C \frac{dv}{dt} \quad (349)$$

we have, for the linear segment of the voltage waveform:

$$I_o = C \frac{\Delta V}{t_c} = C \frac{\Delta V}{DT} \quad (350)$$

from which:

$$\Delta V = \frac{I_o DT}{C} = \frac{V_o DT}{RC} = \frac{V_o D}{fRC} \quad (351)$$

The peak-to-peak output ripple, written in normalized fashion, is:

$$\frac{\Delta V}{V_o} = \frac{D}{fRC} \quad (352)$$

As in the other converters we have examined, the output ripple due to capacitor ESR has been neglected in the previous calculation.

However, for all but the lowest-power converters, the output ripple due to capacitor ESR will dominate.

Output Voltage Sensitivity:

The normalized output voltage is plotted below. For comparison, outputs of the buck converter and the boost converter are plotted also.

As with the boost converter, the buck-boost converter suffers from high sensitivity to duty ratio at high values of D . Thus, operation at high duty ratios generally should be avoided.

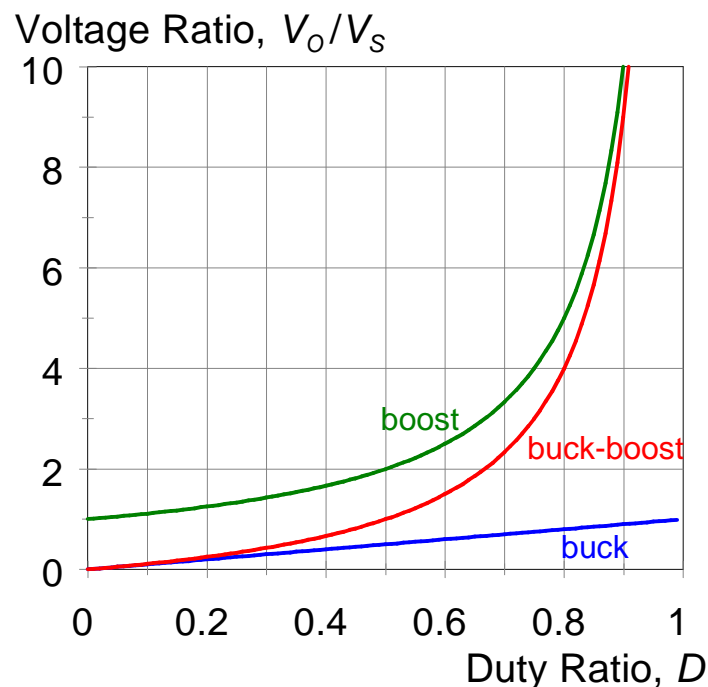


Fig. 323. Normalized output voltage vs. duty ratio for the buck, boost, and buck-boost converters.